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A Complete Analysis and Dynamic Simulations of Superconducting Quantum Interference Device (SQUID) Logic gates

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Abstract

A thorough investigation has been made to obtain SQUID device parameters and properties, and the optimization of the latter for the application of logics gates. SQUID OR, AND gates have been designed theoretically using the optimized techniques. Our concept of turn-on delay has been applied for critically ascertaining the switching speed of these logic gates. The dynamic response of the logics gates have been obtained by computer-simulation. This paper will help for the scientists to have a complete understanding of SQUID logic gates before they are fabricated experimentally to obtain better results.

Keywords

Josephson junction, SQUID, Logic devices, Dynamic simulation

1. Introduction

Josephson junction alone cannot be used as a logic gate since it lacks isolation, i.e., the output signal can propagate in the input as well as in the output branches, whereas for logic operation the signal must propagate only in the output branches. The other problem with this circuit is that the output current is not sufficient to switch more than one load. High-gain Josephson logic devices are desired for many reasons: first, they provide higher fan-out capability (fan-out means the number of loads). Second, high-gain to some extent can be traded off to improve the circuit tolerances from variations in processing parameters such as critical currents. Finally, high-gain would result in shorter gate delays because of the shorter turn-on delays [1]-[4] and the shorter time required for signal currents to reach the device threshold. In practice, a gain of 3 is found to be optimum for Josephson logic circuits. At gains much larger than 3, there is no significant improvements in the gate delay but, on the other hand, the noise margins for the "0" state degrades considerably.

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The Superconducting Quantum Interference Device (SQUID) is a device which can be used for both logic and memory applications. It consists of two Josephson junctions coupled by two inductors. The two most attractive features of SQUID devices for logic applications are isolation and serially connected fan-out. The isolation is provided by the transformer coupling between the SQUID and the input. The other advantage of SQUID is the serial fan-out capability whereby the control lines of many load devices can be connected in series with a single output line.

Before fabricating DC SQUD as a logic and memory device, it is very much necessary to have a thorough understanding and optimization of the device for better results. Earlier i have made an attempt to design DC SQUID as a memory device using computer -simulation method[5].Since the present paper deals with the design of logic gates using the SQUID, it is necessary to have a detailed information regarding the parameters, properties and their optimization for the application of logic and memory cell. In fact, in the present paper we have made an attempt on this line.

2. Brief theory of dc SQUID

The Superconducting Quantum Interference Device (SQUID) is a device which can be used for both logic and memory applications. It consists of two Josephson junctions coupled by two inductors as shown in Fig.1a The two most attractive features of SQUID devices for logic applications are isolation and serially connected fan-out. The isolation is provided by the transformer coupling between the SQUID and the input. The other advantage of SQUID is the serial fan-out capability whereby the control lines of many load devices can be connected in series with a single output line.

An equivalent circuit of SQUID [6] is shown in Fig.2a. When the Josephson junction A and B are assumed to be point junctions, the maximum Josephson current ratio of the junctions A and B is a = I_a/I_b> 1. The total inductance between the

junctions is $L = L_1 + L_2$. The insertion point of the gate current I_g is given by the tap ratio, $p = L_1/L$.

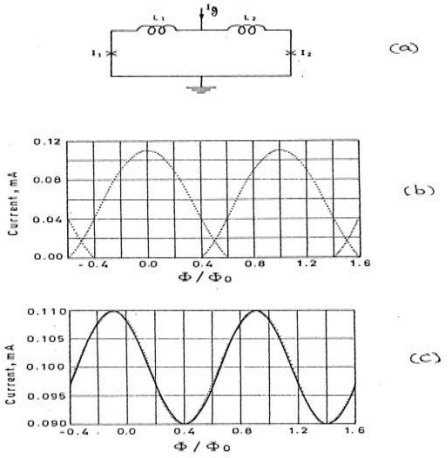

Fig. 1 (a) Diagram of a dc SQUID with bias current. The inductances and junctions on the two sides may be different. The crosses represent the junctions, including resistances and capacitances.(b)The positive half of the threshold characteristic of a symmetric dc SQUID having $L_1 = L_2 = 2.0$ pH and $I_1 = I_2 = 55$ μA.(c) The positive portion of the threshold characteristic of an asymmetric dc SQUID with $L_1 = L_2 = 2.0$ pH and $I_1 = 100$μA ; $I_2 = 10$μA.

The control current I_c represents a transformed control current I_c' of a separate control line. The total flux in the interferometer is an integer multiple N of one flux quantum ϕ_o=2.07 mVps. Flux quantum states (FQS) exist within limited range in the current plane I_g, I_c. Their threshold curves are as functions of phase differences across the junctions θ_a and θ_b:

$I_g = (a. \sin\theta_a + \sin\theta_b) . I_b$ ---------- (1a)

$Ic = [(\theta_a-\theta_b+ 2\pi N) / \lambda-(1- p).\sin\theta_b+ p.a \sin\theta_a].I_b$--- (1b)

$$\theta_b = arc\cos\left(\frac{-a\cos\theta_a}{1+\lambda a\cos\theta_a}\right); a = I_a / I_b ; L = L_1 + L_2$$

$p = L_1 / L$; $\lambda = 2\pi L. I_b / \phi_o$

The curves depend on five magnitude parameters

The characteristic phase $\lambda = 2\pi L I_b/\phi_o$. The maximum Josephson current of the smaller junction I_o

The current ratio, a

The tap ratio, p

The number of flux quanta N.

An example of two FQS in the normalized current plane with $i_G = I_g/I_o$ and $i_C = I_c/I_o$ is given in Fig.3b, for $\lambda = \pi$, a=8, p=0.25 and N=0, 1 [6].

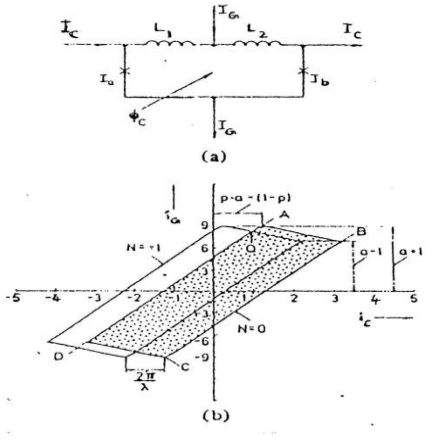

Fig. 2 dc SQUID with two Josephson junctions A and B the total inductance $L = L_1 + L_2$ (a) Equivalent circuit with gate current I_G and the control current I_C. (b) Threshold curves of flux quantum states $I_G = I_G / I_b$ versus $I_C = I_C / I_b$ for a = 8.0, $\lambda = 2\pi$, $p = L_1 / L = 0.25$ and N = -1, 0.

For N = 0 mode, the points A and C are point symmetric with respect to the origin. The same is true for the points B and D. The currents at the points are given analytically [6].

A) $I_{gA} = (a+1) I_o$

$I_{cA} = (p. (a+1) -1). I_o$

B) $I_{gB} = (a-1) I_o$

$I_{cB} (\pi/\lambda + p. (a-1) + 1) I_o$

The control current shift is given by [6]

$\Delta I_c = \phi_o /(L_1 + L_2)$

which can also can be written as

$\Delta I_c = 2\pi I_o/\lambda$

Dynamic response of the SQUID:

In designing Josephson digital circuits, computer simulations of the static as well as of the dynamic device behavior play an essential role because of the lack of sufficiently accurate analytical approximations.

The dynamic description of the superconducting networks, containing Josephson tunnel junctions, self- and mutual -inductances, capacitances and resistors, results in a set of equations for the current continuity and zero-voltage sum and the particular current-voltage integral equations of the junctions. IBM and Bell Labs have been adopting the standard

electrical network analysis programs (for examples ASTAP [7], SPICE [8], etc.) in order to obtain the circuit static as well as the dynamic response [9].

In the present case we have adopted a more general approach to obtain the dynamic response of SQUID. The dynamic equations of the SQUID have been taken and solved numerically by the Runge=Kutta method. In the switching dynamics of a logic gate, the high-frequency oscillation present in the load current with oscillation periods of a few ps stems from the oscillating supercurrent in the interferometer junctions. The frequency of these oscillations is related by to the actual junction voltage. Because these oscillations are still slow enough and can have sufficient energy to switch the following gate, they have to be modeled accurately although the overall switching transient is in the tenths of ps. For an accurate computation of this oscillation, a minimum time-step size in the simulation of about 0.01 has to be used [9].

From Eqns.(10a) and (10b) we can have,
$(1 - P)I_G + I_C = [(\theta_a - \theta_b + 2\pi N)I_o/\lambda + a\, I_o \sin\theta_a]$
In the dynamic case the above equation modifies to:
$(1 - P)I_G + I_C = (\theta_a - \theta_b + 2\pi N)\, I_o /\lambda + a\, I_o \sin\theta_a + a$

$$\frac{\phi_o}{2\pi} C_j \frac{d^2\theta_a}{dt^2} + a \frac{\phi_o}{2\pi R_a} \frac{d\theta_a}{dt}$$

$$or \frac{d^2\theta_a}{dt^2} = \frac{2\pi}{\phi_o C_j a} [(1-p) I_G + I_C + (\frac{\theta_a - \theta_b - 2\pi N}{\lambda}) I_o$$

$$-a\, I_o \sin\theta_a - \frac{a\,\phi_o}{2\pi R_a} \frac{d\theta_a}{dt} \text{ ------ (2)}$$

Similarly,

$$\frac{d^2\theta_b}{dt^2} = \frac{2\pi}{\phi_o\, C_j\, b} [pI_G - I_C + (\frac{\theta_a - \theta_b + 2\pi N}{\lambda}) I_o$$

$$+b\, I_o \sin\theta_b - \frac{b\,\phi_o}{2\pi\, R_b} \frac{d\theta_b}{dt} \text{ --------- (3)}$$

Eqns. (2) and (3) are in the form of the second order differential equation. These equations can be solved by fourth – order Runge-Kutta method on a computer to obtain the dynamic response of the SQUID.

3. SQUID AS AN OR gate

The basic structure of SQUID OR gate is shown in Fig. 6a and its equivalent circuit is given in Fig. 6b. The SQUID OR gate consists of a 2-junction bridge. In designing the SQUID OR gate, it is necessary to obtain threshold characteristic as a function of various device dimensions. The threshold characteristic is calculated by solving equations derived from the equivalent circuits (shown Fig.6b).

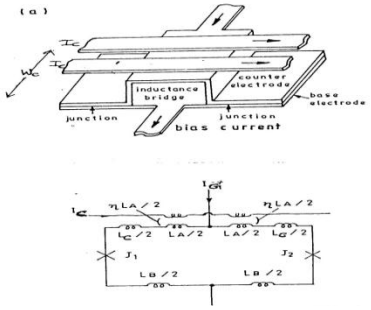

Fig. 3 SQUID and its Equivalent circuit of as a SQUID OR gate

In the calculation, estimated values of inductances in the equivalent circuit play a key role. According to Suzuki [19] the inductances L_A, L_B and L_C are given by

$L_A = \mu_o [(d_{12} + \lambda_{eff})^1 + \lambda_{eff}\, l_J]/K\, Wc$
$L_B = \mu_o \lambda_B (1 + l_j)/[K\, Wc \sinh (d_B/\lambda_B)]$ (4)
$L_C = \mu_o \lambda_C (1 + l_j)/[K\, Wc \sinh(d_C/\lambda_C)]$

where l is the bridge length, l_J is the junction length, Wc is the counter electrode width, d_{12} is the thickness of the insulating layer, K is the fringing factor calculated by given [10], d and dC are the base and counter electrode respectively, and u_o is the permeability.

Here λeff is the sum of the effective London penetration depth of both electrodes, and is given by

$\lambda_{eff} = \lambda_B \tanh (d_B/2\, \lambda_B) + \lambda_C \tanh (d_C/2\, \lambda_C)$

The loop inductance L_{loop} is the sum of L_A, L_B and L_C, and is given by

$L_{loop} = L_A + L_B + L_C = \mu_o [(d_{12} + \lambda loop)\, 1 + \lambda loop\, l_J]/K\, Wc$ and

$\lambda_{1oop} = \lambda_B \coth (d_B/\lambda_B) + \lambda_C \coth (d_C/\lambda_C)$

(K, fringing factor, approximately equal to (1 + 4 d_{12}/W) where .W > > d_{12}) For a 2.5 μm Josephson junction technology, the material parameters used for designing the SQUID OR gate .

Further, the SQUID OR gate is designed under the following conditions:

Line width and line spacing = 2μm

Layer-to-Layer registration = 1.5μm.

With Wc = 7.0μm the device area of the SQUID OR gate is 7μm x 16.5μm.

$p = L_1/L = 0.5$ and $\lambda = 1.01\, \pi$ (approximately).

Dynamic response:

The dynamic response of the designed SQUID OR gate is obtained by substituting the values of device parameters in Eqns. (2) and (3) and solving them by using the fourth-order Runge-Kutta method on a computer.

In Fig.4 the dynamic response of the designed SQUID OR gate has been obtained for two different technologies. The solid curve shows the output current (load) variation of the SQUID OR gate with time using Pb-alloy technology whereas the dotted curve is obtained from Nb/A10 x/Nb Josephson junction base SQUID OR gate. It is apparent from the simulation that the Nb/A10x/Nb base SQUID OR gate has better features over Pb-alloy based OR gate.

Using our concept of the turn-on delay of the Josephson junction [11], the turn-on delay of the SQUID OR gate has been obtained. We have considered the turn-on delay of the SQUID as the time needed for the output phase of the SQUID to reach its phase $\pi/2$.

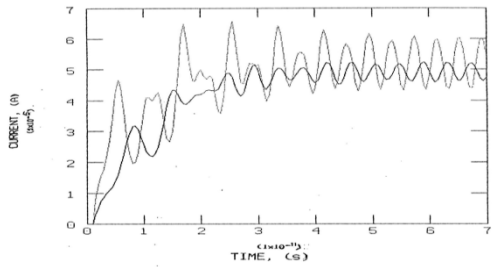

Fig. 4 Dynamic response of a SQUID OR gate using two different technologies. The solid curve shows the output current of Pb-alloy based OR gate with time, whereas the dotted curve indicates the output current variation with time for Nb/A10x/Nb based OR gate.

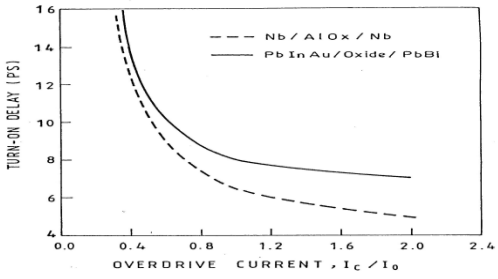

Fig. 5 The turn-on delay of a SQUID OR gate dependence on overdrive current. The solid curve indicates the turn-on delay vs overdrive for a Pb-alloy based OR gate, whereas the dotted curve shows the turn-on delay vs overdrive for a Nb/A10x/Nb based OR gate.

In Fig.5, we have shown the turn-on delay of a SQUID logic gate dependence on the overdrive current. The solid curve indicates the turn-on delay vs overdrive curve for a Pb-ally based SQUID OR gate, whereas the dotted curve is the turn-on delay vs time one for a Nb/A10x/Nb based SQUID OR gate. It can be observed from the figure that the turn-on delay for a Pb-alloy based SQUID OR gate is higher than the Nb/A10 x/Nb based OR gate. This because of the low junction capacitance (0.37pF) in the case of Nb/A10x/Nb based OR gate.

4. SQUID as an AND gate

Asymmetric interferometers with two Josephson junctions or asymmetric dc SQUIDS are very promising devices for digital logic gates. Logic circuits based on these SQUIDS have been investigated [1] [4] . An asymmetric AND interferometer using 3-junctions interferometer have been discussed [12]. In general 3-junction interferometers are used for logic gates whereas 2-junction interferometers are used for the memory application although 3-junction interferometers have better gain tolerances than 2-junction interferometer [13] we have considered 2-junction interferometers for realizing logic gates.

Further, the 2-junction interferometers are simpler and occupy less space compared to 3-junction interferometers. The equivalent circuit of a symmetric two Josephson junction interferometer with nonlinear current injection used for the SQUID AND gate is shown in Fig.6. (according to Beha [9]. The interferometer loop consists of the inductance L = L1 + L2 and the Josephson junctions A and B with the maximum Josephson currents in zero currents in zero field I_{ja} = a.I_0 and I_{jb} = b.I_0. A and B are the phases differences of the Josephson Junctions A and B. Analytic expressions for the calculation of the boundaries of flux quantum states-are derived as follows: The flux quantization condition and the Kirchhoff law yield for the current i_{CN} and the gate current i_G as follows

$$i_{CN} = \frac{1}{p\lambda}\,[\theta_a - \theta_b - (1-p)\lambda b \sin\theta_b + 2\pi N] \text{---}$$

(5a)

$$i_G = a\,.\sin\theta_a + b.\sin\theta_b - i_{CN}$$

----- (5b)

$$\lambda = 2\pi\ LI_o / I_o\ ;\ L = L_1 + L_2\ ;\ p = L_1 / L$$

Two interferometer as AND gates to achieve the high gain, large slope and wide tolerances, the device

parameters are p = 1.0 and λ = 0.87π [13]. In the present case we have tried to achieve these parameters. Beha [14] has investigated a high density SQUID structure for NDRO memory cell. We have used the same structure in order to design AND gate.

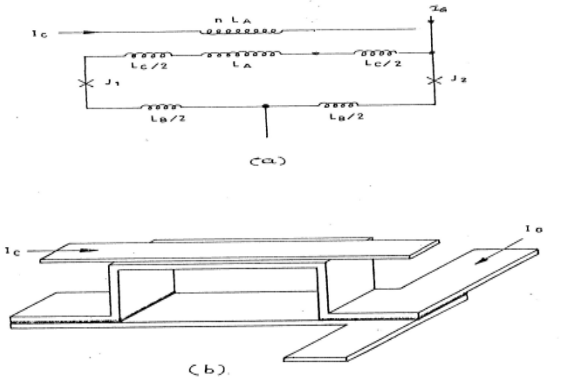

Fig. 6 (a) Equivalent circuit of a SQUID AND gate. b) Static characteristic of the SQUID AND gate. The parameters used for plotting are a = 1.0, b = 3.0, λ = 0.87π and p = L_1 / L = 1.0

Fig. 6a shows the basic structure of the AND gate and Fig.6b shows its equivalent circuit. It can be observed from the two structures (Fig 6a) that there is only one difference in the current injection. Except this the two structures are identical. The device parameters obtained are similar to SQUID OR gate. The device parameters are p = L_1/L = 1.0 and λ = 1.0 π (approximately) have been obtained .For the SQUID AND gate with Wc = 3.5μm, the area of the gate becomes 3.5μm x 16.5μm. The is a very small dimension of the AND gate.

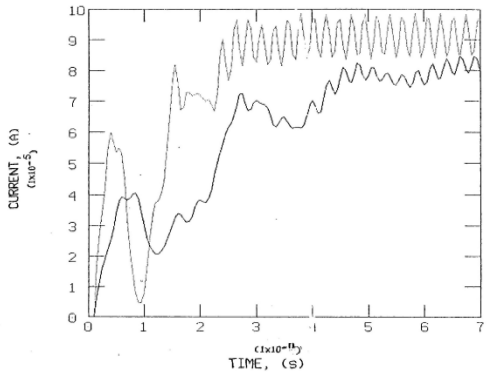

Fig. 7 Dynamic response of a SQUID AND gate using two different technologies. The solid curve shows the output current of Pb-alloy based AND gate with time, whereas the dotted curve indicates the output current variation with time for a Nb/A10x/Nb based AND gate.

In Fig.7 the dynamic response of the designed SQUID AND gate has been obtained for two different technologies. The solid curve shows the output current (load) variation of the SQUID AND gate with time using Pb-alloy technology whereas the dotted curve is obtained from Nb/A10x/Nb Josephson junction based SQUID AND gate. It is apparent from the simulation that the Nb/A10 x/Nb base SQUID AND gate has better features over Pb-alloy based AND gate.

5. Conclusions

In the present paper we have made an attempt to obtain the optimized parameters, properties and optimizations techniques of SQUID to be useful for the design of logics and memory cells. For logic and memory applications, it is found that the optimized device parameters are p = 0.5and λ = π. However, for the SQUID used as an AND gate, the device parameters are obtained as p = 1.0 and λ = π, so that i t provides large gain and operating margins. The logic and memory cell have been designed using these optimized techniques and the dynamic response of these have been obtained by computer-simulation. It is apparent from the simulation that the speed of the designed logic and memory cell is extremely high compared to earlier investigations. Further, the circuit dimension of the logic and memory cell is very low.

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