International Journal of Advanced Computer Research (ISSN (print): 2249-7277 ISSN (online): 2277-7970)
Volume-3 Number-3 Issue-11 September-2013

To Develop Prototype Model of FPGA and RF UP Converter

Neeta S. Matti[1], Saroja V. Siddamal[2]

Abstract

Radio jamming is the transmission of radio signals that disrupt communications by decreasing the signal to noise ratio. RF Jammers are devices designed to prevent other communication devices from successfully operating. RF UP converters are integrated assemblies that convert higher frequency signals to microwave frequencies. The Project work presented here is to develop the prototype model of RF UP converter and FPGA module to disrupt the communication. RF UP converter includes LMK04806 clock conditioner and DAC3484 devices. The frequency data for the RF UP converter is fed from the XC6VLX240T-1FFG1156 because this FPGA has an additional peripheral feature of FMC HPC. The peripherals interfaced with this FPGA on custom board are DDR3 SDRAM, Platform Flash, System Monitor, FMC HPC and Ethernet. The use of FPGA encourages design reuse and can greatly enhance the upgradability of digital systems. To test the peripherals on custom FPGA board and to configure RF UP converter devices, Xilinx 13.4 platform is being used. Tools like Embedded Development Kit and Software Development Kit are used to verify the functionality of the peripherals.
The configuration of LMK04806 and DAC3484 are done using codeloader4 and DAC348x GUI tools respectively.

Keywords

RF Jammer, DDR3 SDRAM, Platform Flash, FMC, LMK04806, DAC3484.

1. Introduction

There are many jammers that prevent cellular communication within the range of the device. Jammers interrupt communication by broadcasting radio transmissions on the particular frequencies used by the targeted devices.

Neeta Matti, Department of Electronics & Communication, BVB Engineering College, Hubli, Karnataka, India.

Saroja V. Siddamal, Department of Electronics & Communication, BVB Engineering College, Hubli, Karnataka, India.

Cell phone jammers are often used for example to prevent the use of cellular telephones in a given area. They do this by generating disruptive signals on the frequencies used by cell phones to communicate with cellular antenna towers. Cell phone jammers can generate disruptive signals upto MHz frequencies.

The main goal of this project is to develop RF UP converter and FPGA modules. The RF UP Converter module is responsible for generating RF signal and up converting the RF signal which is used for jamming signals upto GHz range. This module uses DAC3484 digital to analog converter to transmit the analog signals for jamming. Along with this it also contains LMK04806 clock conditioner to generate the frequencies required by DAC3484. The FPGA module is responsible for generation of digital data for DAC3484 through LVDS interface using FMC connector. The RF UP converter is stacked over FPGA board for being used as RF jammer. As the FPGA board do not have an integrated serial port, it is further interfaced to an external UART for displaying the text messages on HyperTerminal.

2. Literature Review

In 2005, P. B. Kenington[1] proposed the most simple and the most ideal SDR transmitter which consist only of digital signal processing and a high-speed, high resolution, high output power digital to analog converter directly drives the antenna. The ideal receiver would have a similar architecture; an analog-to digital converter would pick up the received signal directly after the antenna, all subsequent signal processing would be done in the digital domain. This kind of system would be ultimately flexible and reconfigurable for different communication standards. However, the ADC and DAC would have to operate at a multiple of the RF carrier frequency to fulfil the Nyquist criterion. Also, a huge dynamic range and, as a result, a very high resolution of the converter is needed. With today's technology, converters with a performance that is good enough to achieve such a system are not (yet) feasible.

In 2006-07, A. Jerng and C. Sodini [2] proposed the RF-DAC architecture which combines D/A-converter

and mixer in a single building block. As this architecture still features a mixer, the digital blocks do not have to operate at a multiple of the carrier frequency. Analog baseband circuitry can be replaced with digital, programmable blocks. One problematic design issue is to distribute the mixing signal to multiple unit sources and maintaining matching and skew.

In 2012, Muralikrishna.B and Gnana Deepika.K [3] proposed that FPGA architectures and performance also evolved so much, so it's the ideal way to drive those very high performance DACs. Among the main FPGA improvements necessary for this kind of applications is I/O SERDES for high speed data transfer required to drive such DACs. For higher channel count, this paper recommends using the Virtex-6, high density/high performance FPGA family with the DAC3484 and LMK04806. In this case, the DAC can work at 2.5 Gs/s to cover the band 50 MHz to 3 GHz.

3. Custom FPGA Board

The custom FPGA Board uses XC6VLX240T-1FFG1156 Virtex-6 FPGA. The Virtex-6 family provides the newest, most advanced features in the FPGA market. The FPGA board provides features common to many embedded processing systems. A high level block diagram of the custom FPGA board and its peripherals is as shown in figure 1. There are 16 I/O banks available on the Virtex-6 device. The bitstream is loaded each time into the device through special configuration pins [4]. These configuration pins serve as the interface for a number of different configuration modes:

- Slave SelectMAP configuration mode
- JTAG/Boundary scan configuration mode
- Byte Peripheral Interface (BPI) flash configuration mode

The specific configuration mode is selected by setting the appropriate level on the dedicated mode input pins M [2:0] of the DIP switch SW1. The M2, M1 and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors (4.7 k), or tied directly to ground. The mode pins should not be toggled before or during configuration, but they can be toggled after configuration [5].

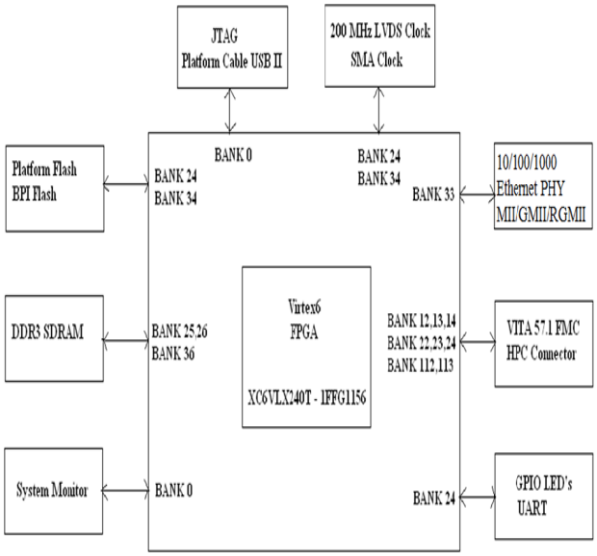

Figure 1: Custom FPGA Block Diagram

3.1 FMC Connector

The custom FPGA board implements High Pin Count (HPC) connector options of VITA 57.1.1 FMC specification. The FMC standard was created to provide a standard mezzanine card form factor, connectors and modular interface to an FPGA located on a base board. The FMC standard defines both a single-width (69 mm x 76.5 mm) and doublewidth (139 mm x 76.5 mm) form factor. The single-width module supports a single connector to the carrier. The double-width module is designed for applications requiring additional bandwidth, more front panel space, or a larger PCB area and supports up to two connectors. The HPC version is fully populated with 400 pins out of which 160 are user-defined, single-ended signals (or 80 user-defined, differential pairs), 10 serial transceiver pairs and additional clocks [5].

3.2 Platform Flash XL

Platform Flash XL is the industry's highest performing configuration and storage device and is specially optimized for high-performance FPGA configuration. Platform Flash XL integrates 128 Mb of in-system programmable flash storage and performance features for configuration within a smallfootprint FT64 package. Platform Flash XL is a non-volatile flash storage solution, optimized for FPGA configuration. The device provides a READY WAIT signal that synchronizes the start of the FPGA configuration process, improving both system reliability and simplifying board design. A wide, 16-bit data bus delivers the FPGA configuration

bitstream at speeds up to 800 Mb/s without wait states. Platform Flash XL is a single-chip configuration solution with additional system-level capabilities. Neither a neither standard NOR flash interface nor supports for common flash interface (CFI) queries provide industry-standard access to the device memory space. The Platform Flash XL's 128 Mb capacity can typically hold one or more FPGA bitstreams. Any memory space not used for bitstream storage can be used to hold general purpose data or embedded processor code [6].

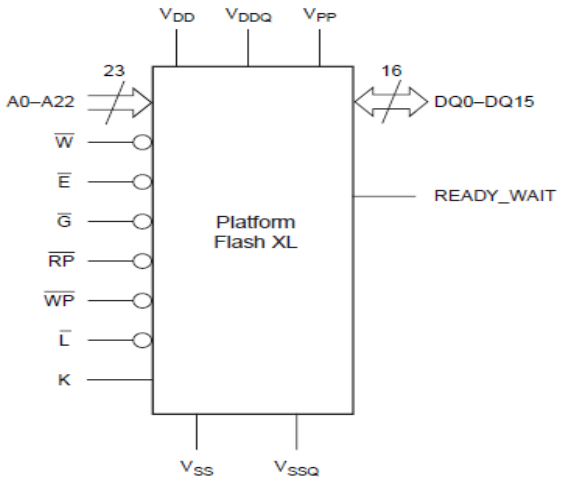

Figure 2: Platform Flash XL Block Diagram

The device is in-system programmable with a 1.8V core power supply (V_{DD}). A separate 3.3V I/O power supply (V_{DDQ}) enables I/O operation at 3.3V. The block diagram of platform flash is as shown in figure 2.

3.3 DDR3 SDRAM

The DDR3 SDRAM is a high speed synchronous dynamic random access memory with eight banks. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. According to JEDEC standards DDR3 runs at a frequency between 800 MHz to 1666 MHz, which is double that of frequency of DDR2. The associated interface techniques used by DDR3 SDRAM is not directly compatible with any earlier type of random access memory due to different signalling voltages, timings, and other factors. The primary benefit of DDR3 SDRAM over its immediate predecessor, DDR2 SDRAM, is its ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth or peak data rates. In addition, the DDR3 standard permits chip capacities of up to 8 gigabits [7].

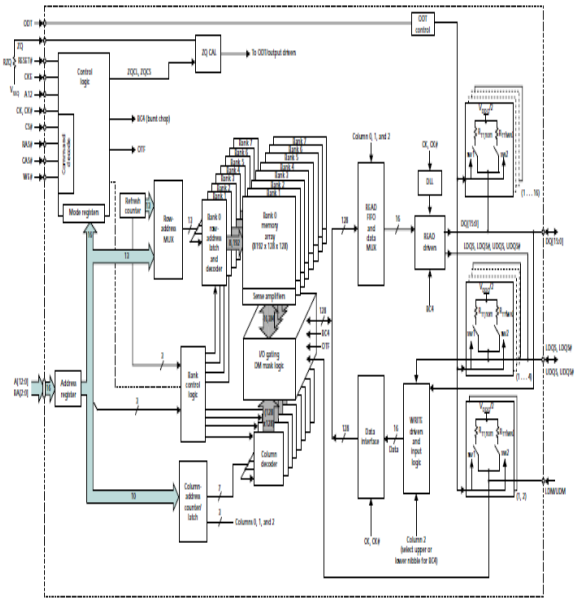

Figure 3: DDR3 SDRAM Block Diagram

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes. The DDR3 SDRAM operates from a differential clock (CK and CK#).

The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble [7].

4. RF UP Converter Board

The RF UP Converter module is responsible for generating RF signal and up converting the RF signal. The module consists of clock divider, two four channel RF DACs and two IQ Modulators. The RF DAC will get frequency data through LVDS interface from FPGA module. The RF output from DAC will be up converted in IQ modulator. Figure 4 shows the block diagram of RF UP converter module.

Input Clock signal for LMK04806 is fed from an external signal generator to generate the clock frequencies of 37.5 MHz and 1200 MHz required for triggering of DAC and continuous analog signal generation from DAC respectively. Two 4-channel DACs are used to produce RF signals ranging from 20MHz to 3GHz. The digital data for DAC3484 is fed from LVDS interface of custom FPGA board via FMC connector. DAC3484 gives out the RF signals which are further fed to filters to produce ripple and glitch free RF signals. The two IQ Modulators are used to up convert RF output from DAC.

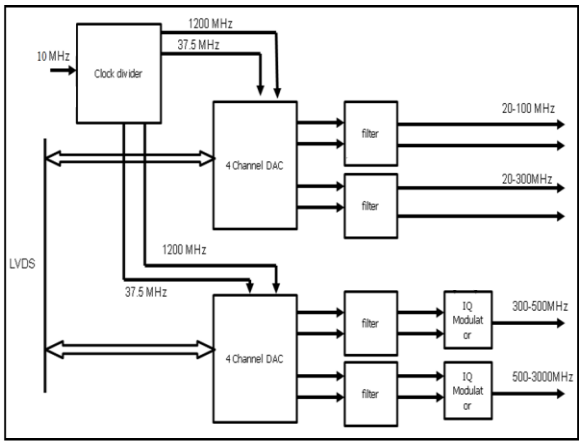

Figure 4: RF UP Converter Block Diagram

4.1 LMK04806 Clock Divider

The LMK04806 is the highest performance clock conditioner with superior clock jitter cleaning, generation and distribution with advanced features to meet next generation system requirements. The clock distribution consists of 6 groups of dividers and delays which drive 12 outputs. All VCO driven outputs have programmable output types. They can be programmed to LVPECL, LVDS or LVCMOS. When all distribution outputs are configured for LVCMOS or single ended LVPECL a total of 24 outputs are available. Each clock group, which is a pair of outputs such as CLKout0 and CLKout1, has a single clock output divider. The divider supports a divide range of 1 to 1045 (even and odd) with 50% output duty cycle. When divides of 26 or greater are used, the divider/delay block uses extended mode. The pin details of the device are as shown in figure 5 [8].

4.2 DAC3484

The DAC3484 is a very low power, high dynamic range, quad-channel, 16-bit digital-to-analog converter with sample rate as high as 1.25 GSPS. The device includes features that simplify the design of complex transmit architectures: 2x to 16x digital interpolation filters with over 90 dB of stop-band attenuation simplify the data interface and reconstruction filters. Digital data is input to the device through a 16-bit LVDS data bus with on-chip termination. The DAC3484 includes a 4-channel, 16-bit wide and 8-samples deep input FIFO which acts as an elastic buffer [9].

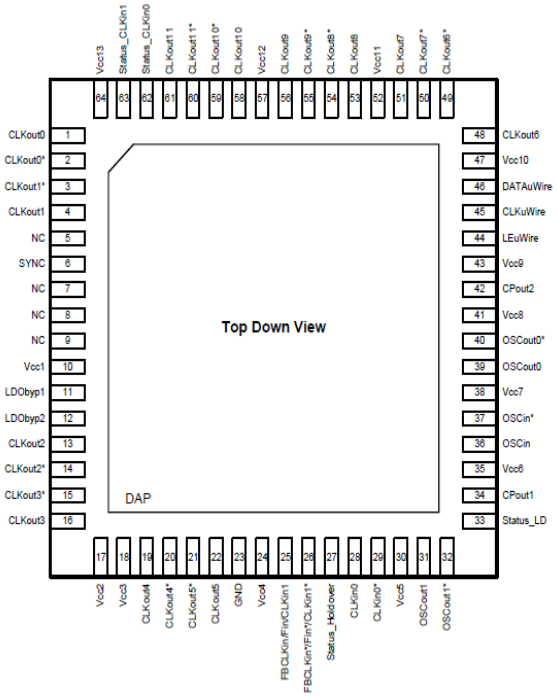

Figure 5: LMK04806 Device

The quad, 16-bit data can be input to the device using either a single-bus, 16-bit interface or a dual-bus, 8 bit interface. The selection between the two modes is done through 16bit in in the config2 register. For both input bus modes, a sync signal, either FRAME or SYNC, can sync the FIFO read and/or write pointers. In byte-wide mode the sync source is needed to establish the correct sample boundaries [9]. The pin details of the DAC3484 are as shown in figure 6.

5. Results

The functionality test of Platform Flash XL and DDR3 SDRAM are being displayed on HyperTerminal. Figure 7 shows the output of Platform Flash. The flash library is initialised and all

the blocks are unlocked. The flash memory contents are erased before writing. The 16-bit data is written to flash as 2 bytes in hexadecimal form with starting address 1FE0000 till 256 locations. Then the same data is being read from flash with same starting address and both the data are compared.

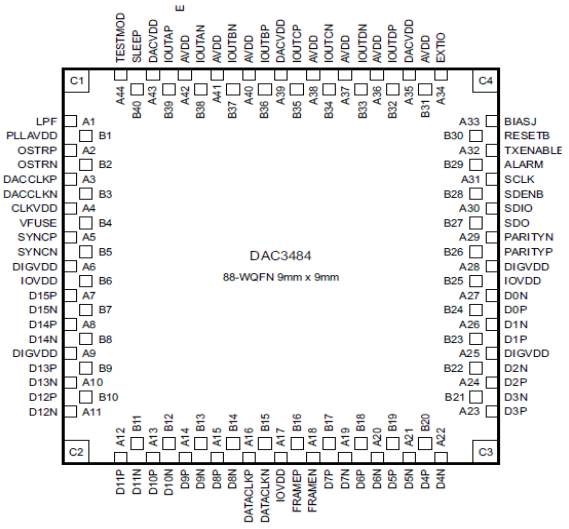

Figure 6: DAC3484 Device

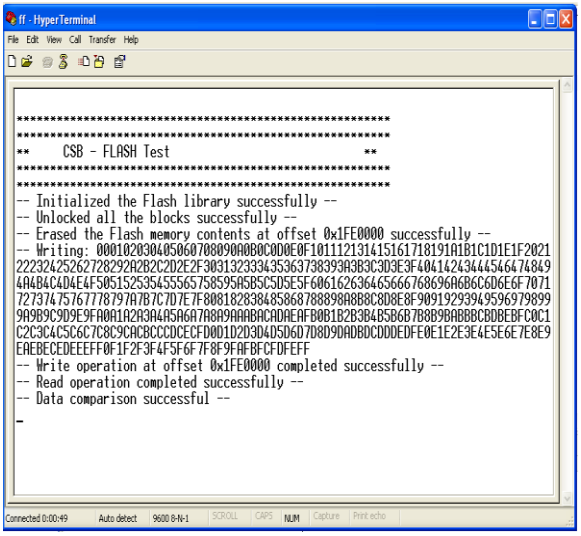

Figure 7: Platform Flash

Figure 8 and 9 shows the output of DDR3 SDRAM. The address range where the data is being written and read is 50200000-5FFFFFFF. Four test cases are written for testing this peripheral. In the first test, a 8-byte zero is being written and read from all the memory addresses. In the second test, a FF is being written and read from all the memory addresses. In the third test, data written to and read from memory are the inverse of their address. For example, if the address is 0011001100110 then the data written on this address is 1100110011001.

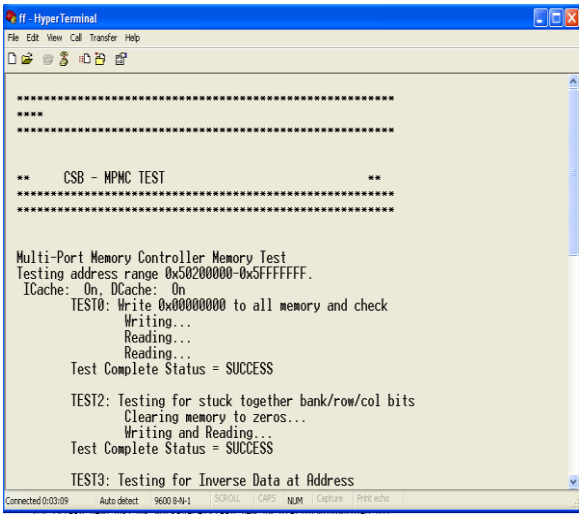

Figure 8: DDR3 SDRAM

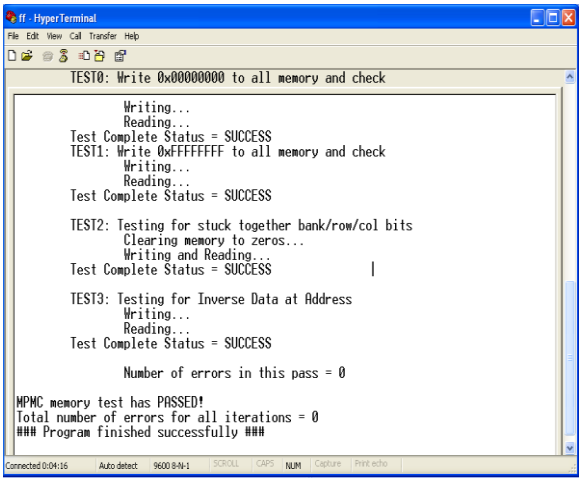

Figure 9: DDR3 SDRAM (Cont.)

Figure 10 shows the simulation output of configuration of LMK04806 and DAC3484 on integrated custom FPGA with RF UP converter board. Here, clkin is the serial clock used by clock conditioner to generate the clocks by LMK04806. Clkoutdac signal is the clock generated by LMK04806 which is fed to the DAC as dac_sclk. At the rising edge of dac_sclk, dacdata is being latched.

The dacdata is the status of each 16-bit register which directly relates to the configuration of DAC3484.

6. Conclusion

The custom FPGA board schematic is studied to know about the board peripherals and their part numbers. By using the part numbers of Platform Flash and DDR3 SDRAM, the background study of these peripherals are carried out to test their functionality. To interface UART with the FPGA board, the voltages of UART board and GPIO LED pins of the FPGA board are taken care of. With this collective study, the functionality test of these peripherals is carried out using XPS and SDK tools.

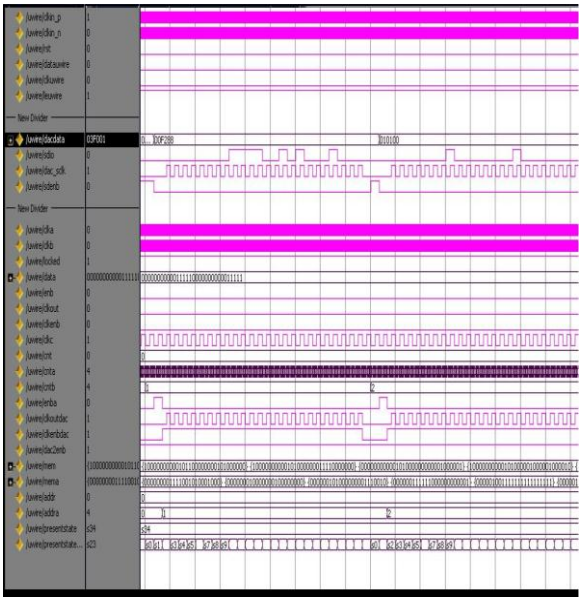

Figure 10: RFDAC Output

The RF UP converter board schematic is studied to know the part numbers of each device on board. By using the part numbers of clock divider and DAC, the background study of LMK04806 and DAC3484 are carried out to configure them. LMK04806 and DAC3484 devices are being configured using CodeLoader 4 and DAC348x tool. The custom FPGA board and RF UP converter board are interfaced via FMC HPC of FPGA board so that the integrated board is used as RF Jammer. The configuration of LMK04806 and DAC3484 is also done by writing a VHDL code and then implemented on integrated board.

In the future, code for the integrated board to be used as RF jammer can be written. Testing of the working of integrated board as RF jammer needs to be performed as this is the main application of this paper. Further, up conversion of signal frequencies can be further extended to 5-6 GHz by AD9739 DAC at the cost of 14 bit resolution.

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Neeta Matti received B.E.(Electronics and Communication) with first class with distinction honours from Visveswaraih Technological University, Belgaum, India in 2010. She is presently pursuing final year M.Tech. from BVB Engineering College(Autonomous), Hubli, India.

Saroja V. Siddamal received BE(Electronics and Communication) with first class honours from Karnataka University, Dharwad, India in 1995. ME(Digital Electronics) from the same university in 1997. She completed her Ph.D. in area of VLSI Signal Processing from JNTU, Hyderabad in 2013. She is presently working as Associate Professor in BVB Engineering College, Hubli, Karnataka. She is the member of ISTE, IETE, scientific and professional societies. Her current areas of research include SOC, VLSI Architecture. She has 3 journal publications and over 15 research papers in International Conference.