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Implementation of Plasmonics in VLSI

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Abstract

This Paper presents the idea of Very Large Scale Integration (VLSI) using Plasmonic Waveguides. Current VLSI techniques are facing challenges with respect to clock frequencies which tend to scale up, making it more difficult for the designers to distribute and maintain low clock skew between these high frequency clocks across the entire chip. Surface Plasmons are light waves that occur at a metal/dielectric interface, where a group of electrons is collectively moving back and forth. These waves are trapped near the surface as they interact with the plasma of electrons near the surface of the metal. The decay length of SPs into the metal is two orders of magnitude smaller than the wavelength of the light in air. This feature of SPs provides the possibility of localization and the guiding of light in sub wavelength metallic structures, and it can be used to construct miniaturized optoelectronic circuits with sub wavelength components. In this paper, various methods of doing the same have been discussed some of which include DLSPPW's, Plasmon waveguides by self-assembly, Silicon-based plasmonic waveguides etc. Hence by using Plasmonic chips, the speed, size and efficiency of microprocessor chips can be revolutionized thus bringing a whole new dimension to VLSI design.

Keywords

Plasmonics, Waveguides, Surface Plasmons

1. Introduction

The electronic chip industry has achieved mammoth amounts of success using VLSI technique for miniaturization of large electronic circuits by integrating billions of transistors and other active and passive elements within a single chip. But today VLSI faces a large limitation w.r.t clock skew rates and lower limit to circuit dimensions. Also, the current copper interconnects used in the electronic circuits pose a major limitation w.r.t data transmission speeds. For example, in the widely used FR-4 copper trace material the loss is approximately 0.5-1.5 dB/in at 5 GHz (Nyquist for 10 Gbps rate), and the loss increases to approximately 2.0-3.0 dB/in at 12.5 GHz (Nyquist for 25 Gbps rate). Return loss and crosstalk can also increase with frequency [1]. Optical fibers have the disadvantage that the guided energy cannot be steered around sharp corners with a bending radius smaller than the wavelength λ of the light [5]. Although light can be guided around sharp corners in photonic crystals, its minimal confinement is nevertheless restricted to the diffraction limit $\lambda/2n$ of the light [4]. The diffraction limit can only be overcome, if the optical mode is somehow converted into a non-radiating mode that is confined to dimensions smaller than the diffraction limit. A possible solution to all the above stated limitations is an all-Plasmonic circuit.

Plasma, the fourth state of matter contains s free positive and negative ions. In response to irradiated light an electron cloud oscillation takes place in metal and semiconductor. Thus just like photon is a quantization of light, Plasmon is a quasi-particle which is a result of quantization of plasma oscillations. Thus, Plasmonics is the science of oscillation of electron cloud in which the frequency of the cloud is equal to that of the irradiated light. Plasmonics is mainly made up of two parts: 1) Surface Plasmon polaritons (SPP) and 2) localize plasmons (LP). The energy required for sending and receiving an SP pulse is much less than the amount needed for charging of a metal wire. This property of the SP does allow them to carry information within a microprocessor with a very high bit rate. This, combined with Plasmonic interconnects made up of Plasmon-based waveguides would result in a much smaller and extremely fast microchip which is not hindered by the diffraction limit, thus giving a major boom to the VLSI technology.

2. Plasmonic Waveguides

Silicon-based Plasmonic Waveguides:
The high refractive index of Si assures strong confinement and a very high level of photonic integration with achievable waveguide separations of the order of 10 nm and waveguide bends with 500 nm radius at telecommunication wavelengths. While

using Al and Cu plasmonic material platforms, makes such waveguides fully compatible with existing CMOS fabrication processes. Their potential future in hybrid electronic/photonic chips is further reinforced as various configurations have been shown to compensate SPP propagation loss. The group velocity dispersion of such waveguides allows over 10 Tb/s signal transfer rates [2]. Dielectric Loaded SPP Waveguides (DLSPPW) are formed by a dielectric ridge on the surface of a metal film and can be fabricated by using industry-standard lithographic processes. In it, the plasmonic signals can be controlled by modifying the properties of the dielectric which is forming the waveguide. The following figure shows the Si-SPP modes in the waveguides of different cross-sections.

When width of the waveguide increases up to 200 nm and higher, the mode becomes more and more localized in the waveguide with its refractive index approaching the refractive index of SPP mode on a plain Si/Al interface.

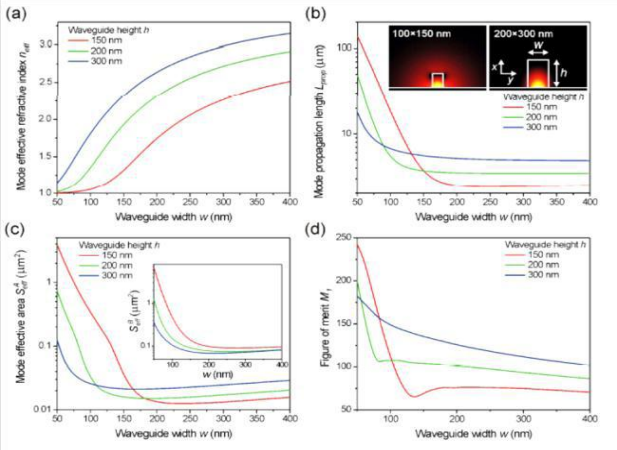

Figure 1. a) Effective refractive index, (b) propagation length, (c) effective area, and (d) figure of merit M1 for Si-SPP mode as a function of waveguide width w and height h. Insets: Field maps presenting the absolute value of the power flow along the waveguide for waveguide cross-sections of 100 × 150 nm2 and 200 × 300 nm2.[2]

The sharpness of waveguide bending is determined by the amount of contrast between the mode refractive index and the refractive index of the surrounding media, which in this case is quite high (Fig. 1b). The following figure shows the output of practical implementation of Silicon based waveguides in nanophotonic circuits. In order to compare various metallic material platforms for Si-based DLSPPWs the waveguide guiding properties have been studied for the case of Au, Al, and Cu [2].

From Fig. 2 it can be concluded that copper is inferior to gold and aluminum in terms of plasmonic properties. Although it provides the highest effective refractive index and the smallest mode area, high Ohmic losses significantly reduce the figure of merit. On the other hand, for the wide range of waveguide cross-sections, the plasmonic properties of aluminum are very similar to those of gold. This makes it a promising candidate for the metallic component of Si-based SPP waveguide circuitry [2]. Silicon has a high refractive index which leads to the sub-wavelength localization of the photonic signal. This property also leads to a sharp waveguide bending which is important for photonic integration. As compared to the conventional Si based waveguides, the propagation length of the mode is inferior but for the design of photonic circuits, it is of utmost importance how strongly the signal is confined within the waveguide and the effect of external stimuli on that during propagation. DLSPPW's are simpler to integrate in CMOS technology and other types of plasmonic waveguide with comparable figures of merit.

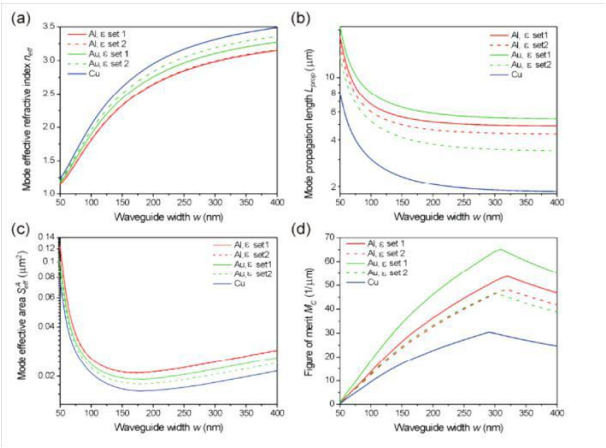

Figure 2. (a) Effective refractive index, (b) propagation length, (c) effective mode area, and (d) figure of merit MC for Si SPP waveguide with height h = 300 nm as a function of its width w for various metals: Au, Al and Cu [2].

Plasmon Waveguides by Self-assembly:

In this method of constructing plasmon waveguides can be carried out by using metal nanoparticle arrays. For efficient dipole coupling of plasmons, the

interparticle should be small, e.g. In case of 50 nm-diameter particles an Interparticle distance of 25 nm is preferred [3]. In a self-assembly method, the nanoparticle arrays are fabricated using template-assisted self assembly of colloids which is an integration of lithography and self- assembly. Wet-chemically synthesized nanoparticles of silica and gold are self assembled into the channels and holes to form arrays composed of 2-15 particles. Using core-shell colloids the interparticle distance in the Au particle array could be controlled by the thickness of the silica-shell [3].

Plasmon waveguides consisting of metal nanoparticles can be fabricated using several methods. A few of the most promising are: (1) electron-beam lithography and lift-off; (2) electron/ion-beam induced deposition (EBID/IBID); (3) colloidal self-assembly. Using the first technique, plasmon waveguides have been successfully fabricated, and electromagnetic energy transport below the diffraction limit has been detected [4]. This method suffers from serious size-limitations, however. For efficient dipole coupling of the plasmons the interparticle distance must be small: in case of 50 nmdiameter particles an interparticle distance of 25 nm is preferred. Such structures are very difficult to fabricate using conventional electron-beam lithography and lift-off techniques. In EBID or IBID, metal nanoparticles are formed by electron-beam induced decomposition of a metallo-organic gas.

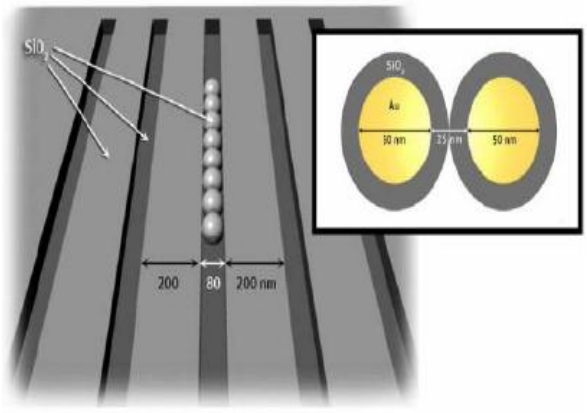

Figure 3. Schematic example of a plasmon waveguide formed by self-assembly of Au core silica-shell colloids in electron beam defined trenches in silica. The inset shows a cross-section of two particles in the waveguide [4]

Using this technique, nanoparticles can be deposited with lateral sizes of 20-30 nm and an interparticle distance of ~10nm [4]. Drawbacks of this technique are the high equipment costs and slow fabrication. Colloidal self-assembly offers some great advantages over these techniques in terms of particle dimensions, fabrication time and costs, although the process is less controllable. Using this method, plasmon waveguides are formed by controlled drying of a colloidal dispersion over a electron-beam patterned substrate. By coating the metal particles with a dielectric material like silica, the Interparticle distance in the particle array can be accurately tuned via the thickness of the shell [3].

Dielectric Loaded SPP Waveguides:

This method of constructing plasmon waveguides has its principal rooted in the dependence of SPP propagation constant on the dielectric refractive index. It basically consists of depositing narrow dielectric ridges on the metal surface. The resulting technology is known as Dielectric Loaded SPP Waveguides (DLSPPW's) and provides an alternate attractive fabrication technology by being compatible with different dielectrics and industrial fabrication method of UV lithography. DLSPPW's provide strong mode confinement and relatively low propagation loss [6].

In fiber coupled waveguide DLSPPW based waveguide structures, intermediate tapered dielectric waveguides were used to funnel the radiation to and from the plasmonic waveguides. The waveguide structures, consisting of 1-μm-thick polymer ridges tapered from 10-μm-wide ridges get deposited directly on a magnesium fluoride substrate to 1-μm-wide ridges placed on a 50-nm-thick and 100-μmwide gold stripe. These are fabricated by large-scale UV-lithography.

DLSPPWs have been characterized demonstrating the overall insertion loss below 24 dB, half of which was attributed to the DLSPPW loss of propagation over the 100 μm-long distance [6]. The advantage of DLSPPWs compared to other SPP waveguide types is that a dielectric ridge can be easily functionalized to provide thermo-optical, electro-optical, or all-optical functionalities and can be used for the development of active plasmonic components. Moreover, DLSPPWs fabrication is compatible with current lithography process used in the fabrication of electronic circuits.

Combined with intrinsic possibility to control optical signals by electronic ones and vice versa, the DLSPPW's provide an excellent alternative to fast plasmon based waveguides.

3. Conclusion

Thus, this paper puts forward the idea of replacing oft used interconnects with plasmonic waveguides. This would not only help reduce the energy losses during transmission of data using interconnects but also provide an ideal solution to the limitations w.r.t the clock speed, data transmission rates, clock skew rates and circuit size that the current VLSI technology is facing. Also, the technologies mentioned in this paper have been tested and are still been worked upon by various research centres. More, importantly, most of these technologies are compatible with the current CMOS based VLSI techniques used by the industries, thus making their adaptation simpler.

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