International Journal of Advanced Computer Research (ISSN (print): 2249-7277 ISSN (online): 2277-7970)
Volume-2 Number-1 Issue-3 March-2012

Exploring Quantum Dot Cellular Automata Based Reversible Circuit

Saroj Kumar Chandra[1], Deepak Kant Netam[2]
Department of Information Technology & Engineering Institute of Technology Guru Ghasidas Vishwavidyalaya, Bilaspur (Chhattisgarh)[1,2]

Abstract

Quantum-dot Cellular Automata (QCA) is a new technology for development of logic circuits based on nanotechnology, and it is an one of the alternative for designing high performance computing over existing CMOS technology. The basic logic in QCA does not use voltage level for logic representation rather it represent binary state by polarization of electrons on the Quantum Cell which is basic building block of QCA. Extensive work is going on QCA for circuit design due to low power consumption and regularity in the circuit.. Clocking is used in QCA circuit to synchronize and control the information flow and to provide the power to run the circuit. Reversible logic design is a well-known paradigm in digital computation, and if circuit developed is reversible then it consumes very low power. Here, in this paper we are presenting a Reversible Universal Gate (RUG) based on Quantum-dot Cellular Automata (QCA). The RUG implemented by QCA Designer tool and also its behavior is simulated by it.

Keywords

QCA, RUG, QCA Designer, MV, INV

1. Introduction

Due to the miniaturization of transistors, the basic building unit of digital circuits in VLSI technology such as CMOS, the performance of computer chips has shown outstanding development in the last decades. CMOS technology represents binary information by switching the electric current [1] [2] [3] [4]. However, this paradigm has serious drawbacks as device sizes are reduced. The interconnection of devices and signals is one of these problems. Another problem is with regard to the quantization of charge, which becomes significant as transistors become smaller. Finally, current switching results in huge energy dissipation. Recent studies show that the spatial limits of conventional electronics will be reached in the next few years and, as a consequence, this continuing development of VLSI technology is threatened. Thus, new computational paradigms that leverage the quantum effects present in the nanometric scale will have to be approached in order to develop new technologies overcome the barrier imposed by physical laws. The paradigm of Quantum-Dot Cellular Automata (QCA) is one of the most promising alternatives to the CMOS-VLSI technologies [3].

Nanotechnology has been the focus of extensive research in recent years. One of the most pressing hurdles in the development of innovative computation paradigms and systems is energy dissipation [5] [6]. A possible solution is reversible computing. QCA is a promising emerging Nanotechnology that relies on novel design concepts. The basic logic devices for QCA are the majority voter (MV) and inverter (INV) [1]. QCA cells and some simple devices have already been successfully developed [7], [8], [9]. A four-phase clocking scheme for QCA also known as Landauer clocking has been proposed in [10]. Based on this clocking scheme, combinational as well as sequential logic design in QCA has been proposed in [1]. QCA has very low power consumption. So, QCA has been deemed as a promising technology for building reversible systems.

2. QCA Basic Building Block

The basic building-block of QCA devices is the QCA cell. A QCA cell consists of four quantum dots located at corners of the square. When cell is charged with two excess electrons, they occupy diagonal site because of mutual electrostatic repulsion. Due to columbic interaction only two configurations of the electron pair exist and they are stable. Assign a logic 0 and logic 1 to represent the stable (ground) states of the cells. The two electrons that can move to any quantum dot within the cell through electron tunneling. It is assumed that tunneling is fully controllable by potential barriers that can be raised and lowered across neighboring cells. The potential barriers are implemented using capacitive plates. Electrostatic interaction between neighboring cells allows the design of QCA wires, logic devices and even simple microprocessors. The geometry of molecular four-dot QCA cells enables the clocking of

QCA devices via an electric field generated by a layout of clocking wires. Thus precise control over the timing and direction of data flow in QCA circuits is possible. The design of QCA circuits now lies not only in the logic structure of the cells, but also in the layout of clocking wires.

In 0- polarization cells are in the non-polarized state also called NULL state, which is a superposition of the two ACTIVE states and does not represent a binary value. In +1- polarization the cells are in positive Polarized state. This state is considered as Logic-1. In -1- polarization the cells there are in Negative Polarized state. This state is considered as Logic-0 as shown in figure 1.

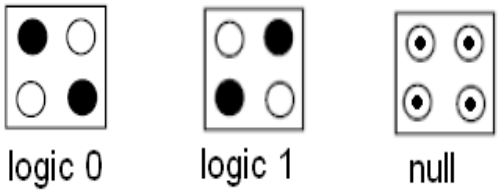

Figure 1: Quantum cells with +1,-1 and null polarization.

A. Majority Voter

The fundamental logic primitive that can be realized in QCA is the majority gate as shown below. A three-input majority function M is logic high if two more of its inputs are logic high. That is M (A, B, C) =AB+BC+CA where A, B and C are arbitrary inputs, can be realized by only five QCA cells (compared to a CMOS implementation, which require sixteen transistor) as shown in figure 2. A QCA majority gate, implements a majority function. A network of majority gates is called a majority network.

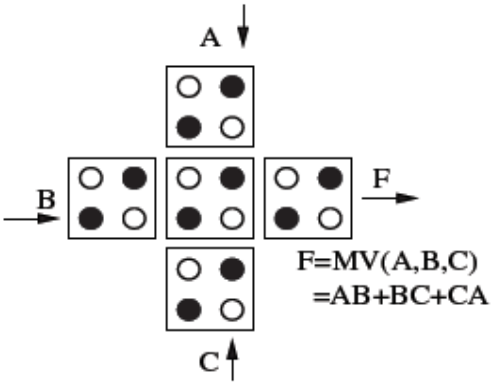

Figure 2: QCA Majority voter

B. Inverter

The implementation of inverter based on QCA is shown in figure 3.

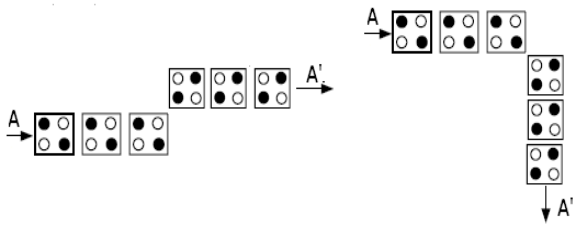

Figure 3: QCA based inverter

3. Reversible Logic

Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system consists of reversible gate. Reversible computing investigates the relation between energy dissipation and computing at logic level, which leads to the thermodynamic limit of computation. Research on reversible logic is not only of theoretical importance, but also of realistic necessity. Reversible computation is accomplished at logic level by establishing a one-to-one onto mapping between the input states and output states of the circuit [11]. This bijective property was initially investigated by Landauer who has proved that the lower bound of heat dissipation for every bit of information lost in computing is kTln2 joules, where k is Boltzmann's constant and T is the temperature. Moreover, dissipation can be avoided if computation is carried out without losing any information. Due to the bijective property, testing of reversible logic is also generally simpler than conventional irreversible logic[12]. Reversible logic gates are information lossless, i.e. the information output of a reversible circuit is maximized. Therefore according to [5], the probability of fault detection is maximized too. Reversible logic is inherently easier to test because the one-to-one onto property improves the controllability as well as the observability of the circuit[14]. New reversible logic gates are defined in QCA by their bijective property, i.e. the one-to-one onto mapping between inputs and outputs. In reversible logic there is one-to-one mapping between the input and output vector and vice- versa. A QCA is one of the possible technologies to implement the reversible logic.

A. Reversible Gate

A logic gate L is reversible if, for any output Y, there is a unique input X such that
$L(X) = Y$

If a gate L is reversible, there is an inverse gate L′ which maps Y to X for which

$$L'(Y) = X.$$

From common logic gates, NOT gate is reversible, as can be seen from its truth table below.

Table 1: Truth Table For Not Gate

INPUT	OUTPUT
0	1
1	0

The original motivation was that reversible gates dissipate less heat (or, in principle, no heat). In a normal gate, input states are lost, since less information is present in the output than was present at the input. This loss of information loses energy to the surrounding area as heat, because of thermodynamic entropy. Another way to understand this is that charges on a circuit are grounded and thus flow away, taking a small charge of energy with them when they change state. A reversible gate only moves the states around, and since no information is lost, so energy is conserved. Any reversible gate must have the same number of input and output bits, by the pigeonhole principle - For one input bit there are two possible reversible gates. One of them is NOT and the other is the identity gate which maps its input to the output unchanged.

B. Existed Reversible Gates

Here we look TWO basic existed revisable gates namely fredkin and Toffoli Gates's,

1). Fredkin Gate: Fredkin gate is one of the most studied reversible gate with 3-inputs and 3-outputs. Fredkin gate produce the same number of 1's in the output as on the input, in addition to the one-to-one mapping feature of reversibility. Its input parity is equals to the output parity, so Fredkin gate is parity preserving [13]. If the 3-input and 3-output for Fredkin gate are A, B, C and P,Q,R respectively then it's input and output configuration can be seen as shown in figure 4.

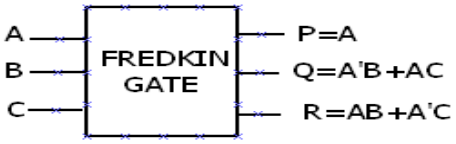

Figure 4: Block diagram of Fredkin Gate

QCA cell layout of the Fredkin Gate is shown in figure 5 using four-phase clocking scheme.

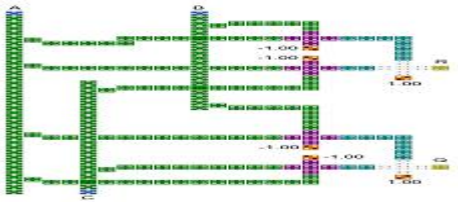

Figure 5: QCA layout of Fredkin Gate

2). Toffoli Gate : Toffoli Gate has a 3-bit input and 3-bit output. If the first two bits are set, it flips the third bit. The output of Toffoli gate can be described as mapping bits A, B and C to A, B and C XOR (A AND B) as shown in figure 6. The Toffoli gate is universal; this means that for any Boolean function one can use Toffoli gates to build systems that will perform any desired Boolean function computation in a reversible manner.

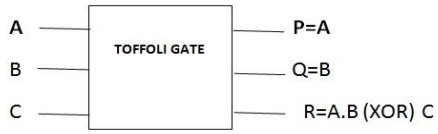

Figure 6: Block diagram of Toffoli Gate

QCA realization of the Toffoli Gate using only majority gate is shown in figure 7.

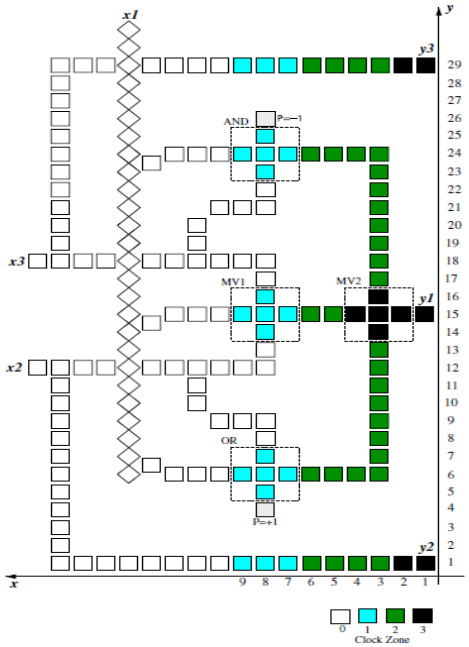

Figure 7: QCA layout of Toffoli Gate

4. Reversible Universal Gate (RUG)

Reversible Universal Gate has a 3-bit input and 3-bit output. First output is majority function, second output is Universal function and its third output is XOR function. The output of RUG gate can be described as mapping bits A,B and C to AB+BC+CA, AB+A'C' and B'C+BC' respectively as shown in figure 8.

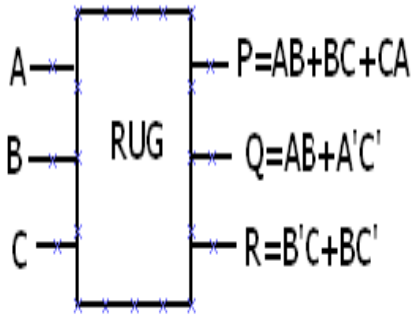

Figure 8: Block Diagram of RUG Gate

The RUG gate is universal; this means that for any Boolean function f($x_1, x_2, x_3, \ldots\ldots x_m$), there is a circuit consisting of RUG gates which takes $x_1, x_2, x_3, \ldots\ldots x_m$ and some extra bits set to 0 or 1 and outputs $x_1, x_2, x_3, \ldots\ldots x_m$, f($x_1, x_2, x_3, \ldots\ldots x_m$), and some extra bits. Essentially, this means that one can use RUG gates to build systems that will perform any desired Boolean function computation in a reversible manner QCA cell layout of the RUG is shown in figure 9 using four-phase clocking scheme

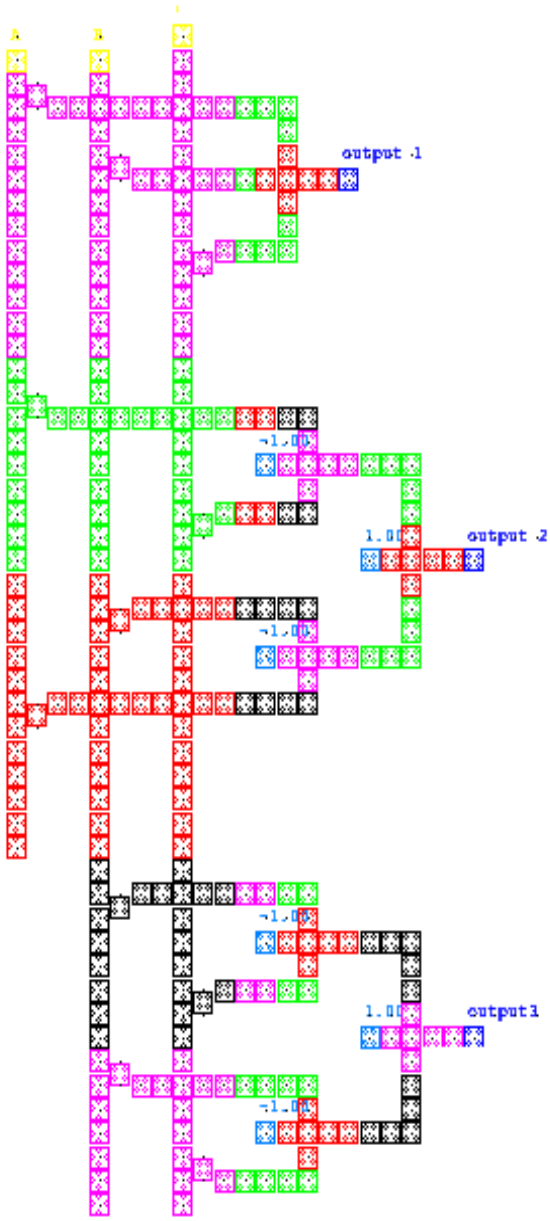

Figure 9: QCA layout of RUG Gate

RUG logic design is consist of seven majority gates (MV) and four inverter, as shown in figure 9 retains the simple clocking scheme. For the wire A, B, C it is in different clock zone because to main signal strength. Similarly all MV's also kept in corresponding clock zones.

Output OF RUG Gate using QCADesigner of is shown in figure 10 using four-phase clocking.

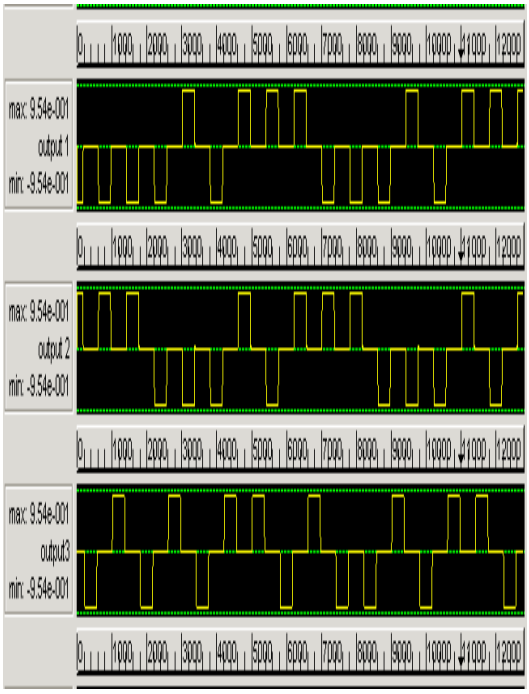

Figure 10: Output of RUG Gate using QCA Designer.

A Universal Function is a function which can achieve any logic with a given number of variables with minimum number of wire crossings [14]. So from [14], presence of universal function RUG based QCA circuits are very much cost-effective in terms of number of logic gate, wire crossing, cells count as compared to the designs based on existing reversible gate. This is the concept of a special form of reversible logic with universal functionality.

5. Conclusion

RUG is a 3X3 input output reversible logic gate having majority function and universal function and XOR function as outputs and A, B, C are its inputs respectively. RUG gate can realize all standard functions as well as symmetric function with better cost-effective results in terms of number of logic gate, wire crossings, cells count as compared to the designs based on existing reversible gates. Like any other reversible gates RUG do not erase information and ultimately it leads high performance computing.

Acknowledgment

We are thankful to Mr. Bibhas Sen (Assistant Professor), Department of Computer Science & Engineering, National Institute of technology, Durgapur (W.B) for constant guidance and encouragement.

References

[1] P.Tougaw and C.Lent, “Logical Devices Implemented using Quantum Cellular Automata”, Journal of Applied Physics, vol.75, no.3, pp.1818-1825, 1994.

[2] C.S.Lent and P.D.Tougaw,”A Device Architecture for Computing with Quantum Dots,” Proc.IEEE, vol.85, no.4, pp.541-577, Apr.1997.

[3] W.Porod , ”Quantum-Dot Devices and Qunatum-Dot Cellualr Automata”, hirer J Bi/urcorionond Cltaor,YO7I.,no.10, pp.2199-2218,1997.

[4] I.Amlani , ”Digital Logic Gate Using Quantum-Dot Cellular Automata”, Science v01.284,pp.289-291,1999.

[5] Lent, Craig S., Mo Liu, and Yuhui Lu. "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling." Nanotechnology 17, no. 16 (2006): 4240.

[6] R.Landaurer, ”Irreversibility and Heat Generation in the Computational Process”, IBM Journal of Research and Development,vol.5,pp 183-191,1961.

[7] Amlani, Islamshah, Alexei O. Orlov, Gregory L. Snider, Craig S. Lent, and Gary H. Bernstein. "Demonstration of a functional quantum-dot cellular automata cell." Journal of Vacuum Science & Technology B 16, no. 6 (1998): 3795-3799.

[8] I.Amlani ,”Digital Logic Gate Using Quantum-Dot Cellular Automata” , Science ,pp.289-291,1999.

[9] G.L. Snider,”Experimental Demonstration of Quantum-Dot Cellular Automata”, Semiconductor Science Technology, vol.13, pp.A130-A134, 1998.

[10] K. Hennessy and C. Lent, “Clocking of Molecular Quantum-Dot Cellular Automata”, Journal Of Vacuum Science and Technology,vol.19,no.5,pp.1752-1755,2001.

[11] C.H. Bennett,” Logic Reversibility of Computation”, IBM Journal of Research and Development, vol.17, pp.525-532, 2004.

[12] K. N. Patel, J. P. Hayes, I. L. Markov, ”Fault Testing For Reversible Circuits,” IEEE Trans. On Computers, vol.30, pp.1220-1230, 2004.

[13] H.Thapliyal, N.Ranganathan “Concurrently Testable FPGA Design for Molecular QCA Using Conservative Reversible Gate”, pp.1815-1818, 2009.

[14] Yinshui Xia, Keming Qui,”Design and Application of Universal Logic Gate Based on Quantum-Dot Cellular Automata”, pp.335-338, 2008.

Saroj Kumar Chandra ,Received his B.E.(I.T.) Degree from Guru Ghasidas University Bilaspur(C.G),India,in 2007, and M.Tech(C.S.E) Degree from National Institute Of technology Durgapur(W.B),India in 2010.Currently working as Assistant professor in Institute Of Technology, Guru Ghasidas University Bilaspur (C.G.) in the Department Of Information Technology.

Deepak Kant Netam ,Received his B.E.(I.T.) Degree from Guru Ghasidas University Bilaspur(C.G),India,in 2008, and M.Tech(C.S.E) Degree from National Institute Of technology Durgapur(W.B),India in 2010.Currently working as Assistant professor in Institute Of Technology, Guru Ghasidas University Bilaspur (C.G.) in the Department Of Information Technology.