

THD Reduction in Performance of Cascaded Multi-Level Inverter Fed Induction Motor Drive

Naveen Kumar Verma¹, Preeti Gupta², Amit Shrivastava³

Abstract

The multilevel inverter power structure plays a vital role in the power industry. It is easier to produce a high-power, high-voltage inverter with the multilevel structure. The topologies of multilevel inverter have several advantages such as lower total harmonic distortion (THD), lower electromagnetic interference (EMI) generation, reduction of voltage ratings of the power semiconductor switching devices and high output voltage. This paper presents a universal control scheme based on multicarrier PWM methods and its implementation in three-level, five-level and nine-level cascaded inverters feeding a three phase induction motor. This paper compares total harmonic distortion values of voltage and current waveforms of induction motors between different levels.

Keywords

Cascaded Multi-level inverter (CMLI), Multicarrier pulse width modulation (MPWM), Three-level Multi level inverter (MLI), Five-level MLI, Nine-level MLI, Induction motor, Total harmonic distortion (THD).

1. Introduction

Application of multilevel voltage source inverter is mainly advantageous in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the important advantages of multilevel configuration is the reduction in the harmonics of output waveform without increasing switching frequency or decreasing the inverter power output [1], [2], [3]. The output voltage waveform of a multilevel inverter comprises of number of levels of voltages, typically obtained from capacitor voltage sources.

The so-called multilevel inverter starts from three levels. As the number of levels increases, the output THD decreases. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Three common topology of multilevel inverters based on capacitor voltage synthesis are proposed as Diode-Clamped Multilevel Inverter, Flying-Capacitor Multilevel Inverter and Cascaded-Inverters with Separated DC Sources.

In this paper, a universal control scheme based on multicarrier PWM methods and its implementation in three-level, five-level and nine-level cascaded inverters feeding a three phase induction motor is presented. Advantage of using cascaded-inverter is circuit layout flexibility. Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitor. The number of output voltage levels can be easily adjusted by adding or removing the full-bridge cells. Modulation topology proposed in this paper is Multicarrier Pulse Width Modulation, which is one of the primitive techniques and is used to suppress harmonics presented in the quasi-square wave. Only triangular carrier is considered in this paper. Simulation studies are carried out using 3-Phase, 50HP, 400V, 50Hz, and 1500 RPM induction machine.

This paper comprises of eight sections. Section 2 describes Literature Survey. Section 3 describes the theory of a cascaded-inverter with separated dc sources. Section 4 describes harmonic elimination in multi-level inverters. Section 5 deals with multicarrier PWM technique. Section 6 presents the Simulation results. Section 7 gives the comparison of percentage THD of different levels of CMLI and finally section 8 will conclude the work.

2. Literature Review

In 2010, Kfir J. Dagan, Raul Rabinovici and Dmitry Baimel [4] proposed an analytical approach to the evaluation of harmonic content in multi-level inverters. An analytical formula is introduced for the

Naveen Kumar Verma, Electrical and Electronics Department, Oriental College of Technology (OCT), Bhopal, Madhya Pradesh.

Preeti Gupta, Electrical and Electronics Department, Oriental College of Technology (OCT), Bhopal, Madhya Pradesh.

Amit Shrivastava, Electrical and Electronics Department, Oriental College of Technology (OCT), Bhopal, Madhya Pradesh.

phase voltage total harmonic distortion (THD) of any multi-level pulse-width modulation (PWM). The proposed formula depends only on fundamental amplitude, inverter's voltage level and switching angles.

In 2011, S.Flora Viji Rose and Mr. B.V. Manikandan [5] proposed Simulation and Implementation of Multilevel Inverter Based Induction Motor Drive. An open loop speed control has been achieved by using v/f method. The proposed system was an effective replacement for the conventional method which produces high switching losses, results in poor drive performance.

In 1996, G. Durgasukumar and M.K. Pathak [6] proposed THD Reduction in Performance of Multi-Level Inverter fed Induction Motor Drive. Application of simplified space vector modulation (SVM) method for different level diode clamped inverter is presented in this paper. SVM offers several advantages such as reduction in execution time and savings in controller memory in case of experimental realization.

3. Literature Review

Cascaded Multilevel Inverter (CMLI) topology is the most advantageous topology in the family of multilevel inverters. It requires less number of components as compared to diode-clamped and flying capacitors type multilevel inverters. It has modular structure with easier switching Strategy and occupies less space [7] - [8]. Fig.1 shows n-level CMLI. The CMLI comprises of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series. Each H-bridge is capable of producing three different voltage levels: +Vdc, 0, and -Vdc by connecting the dc source to ac output side by different combinations of four switches SA1, SA2, SA3 and SA4. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs.

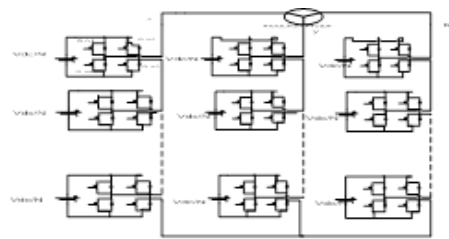


Fig.1 Cascaded n-level multi-level inverter

4. Harmonic Elimination in Multi-Level Inverter

Harmonics are unwanted current or voltage [9]. They exist at some integer multiple or fraction of the fundamental frequency. The harmonics orders and magnitude depend on the inverter topology and the modulation technique, for example in single phase VSI, only odd harmonics are present in the output voltage waveform. The even harmonics are absent due to the half wave symmetry of the output voltage harmonics. For three phase VSI, in addition to the even harmonics triplet (third and multiple of third harmonics) are also absent. The output voltage $V(t)$ as in eqn. 1 of the multi-level inverter can be expressed in Fourier series as:

$$V(t) = \sum_{n=1}^{\infty} (a_n \sin na + b_n \cos na) \dots \dots \text{eqn.(1)}$$

Even harmonics are absent ($b_n = 0$) due to quarter wave symmetry of the output voltage and only odd harmonics are present. The amplitude of the n^{th} harmonic a_n is expressed only with the first quadrant switching angle $\alpha_1, \alpha_2, \alpha_3, \dots, \alpha_m$ as shown in eqn.(2) and (3).

$$a_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^m \cos n\alpha_k \dots \dots \dots \text{eqn.(2)}$$

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \dots < \alpha_m < \pi/2 \dots \dots \dots \text{eqn.(3)}$$

For any odd harmonics can be expressed up to k^{th} term where m is the number of variable corresponding to switching angle α_1 through α_m of the first quadrant. THD expression is shown as in eqn. (4)

$$\text{THD} = \frac{1}{\text{fundamental}} \left[\sum_{n=2}^{\infty} (n^{\text{th}} \text{ harmonic component})^2 \right]^{\frac{1}{2}} \dots \text{eqn (4)}$$

5. Modulation Topology

It is universally accepted that with improved switching strategies, harmonic contents of output voltages can be considerably reduced. Power electronics researchers have studied many novel control techniques to reduce harmonics in output waveform. Space vector and multicarrier PWM techniques are considered as high switching frequency modulation methods [10,11] and active harmonic elimination, selective harmonic elimination and fundamental frequency methods are considered as low switching frequency methods [12]. In the present work, multicarrier PWM scheme is used.

In a multicarrier PWM scheme, carrier signals depending upon number of levels are compared with the reference signal and pulses obtained are given to

switches corresponding to different levels. The reference signal or the modulating signal is a sinusoidal waveform and all the carrier signals are triangular. At every instant, each carrier is compared with the modulating signal. For all the carrier signals above the zero reference, each comparison gives '1' if the modulating signal is greater than the carrier and '0' otherwise. For all the carrier signals below the zero reference, each comparison gives '0' if the modulating signal is greater than the carrier and '-1' otherwise. Above results obtained are added and it is observed that it acquires same wave shape as that of expected output voltage. Fig.2 Shows Simulink model of multicarrier PWM generation for a five level inverter. In this four triangular carriers are compared with a reference sinusoidal waveform. Fig.3 Shows Switching pattern produced using carrier based PWM scheme for a five level inverter and it is observed that it acquires same wave shape as that of expected output voltage.

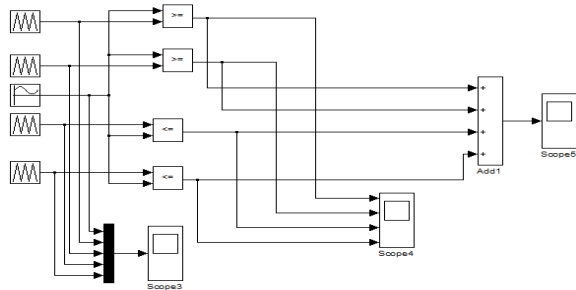


Fig.2 Simulink model of multicarrier PWM generation for a five level inverter.

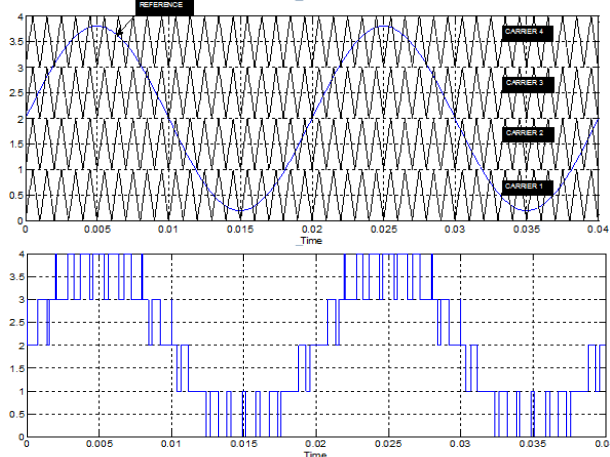


Fig.3 Switching pattern produced using carrier based PWM scheme for a five level inverter

6. Simulation Results

A. Three- level inverter fed induction motor

Fig.4 shows the simulink model of 3-level inverter fed induction motor drive. Three-level inverter is modelled based on the theoretical concepts explained in chapter 3. Switching pattern produced for a three level inverter comprises of two triangular carrier and a reference sinusoidal waveform. Four pulses are generated which are given to the four switches of one leg of three level inverter. Similarly the pulses are generated for remaining phases. Modulating signal is phase shifted by 120 degrees. The corresponding line-line voltages and the performance parameter speed, torque, currents and total harmonic distortion are shown in fig.5-10.

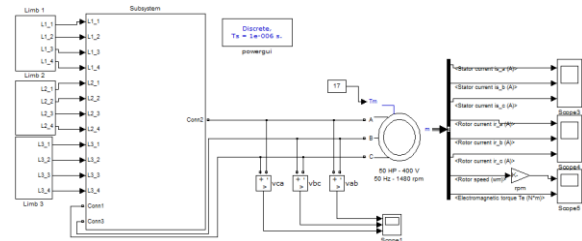


Fig.4 simulation circuit of Three level MLI

1. Line voltages

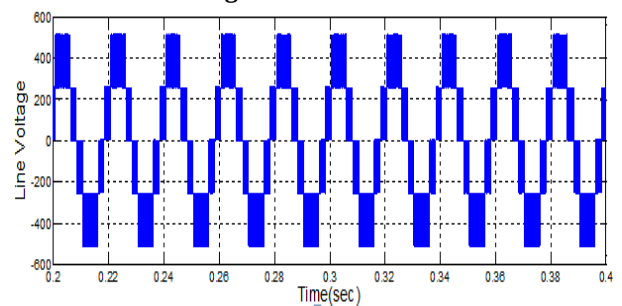


Fig.5 Three level inverter line-line voltages

2. Performance parameter of induction motor

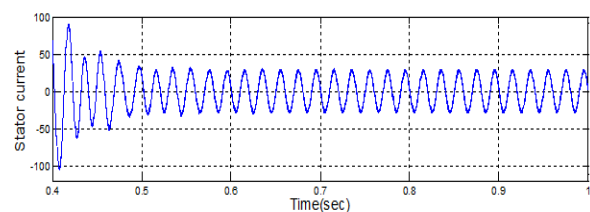


Fig.6 Stator current of 3-level inverter

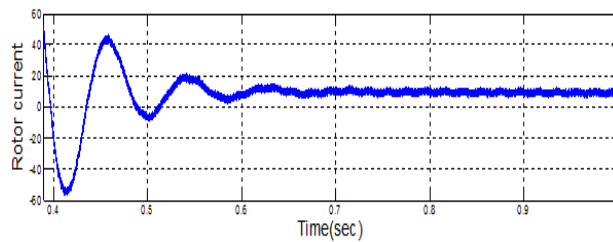


Fig.7 Rotor current of 3-level inverter

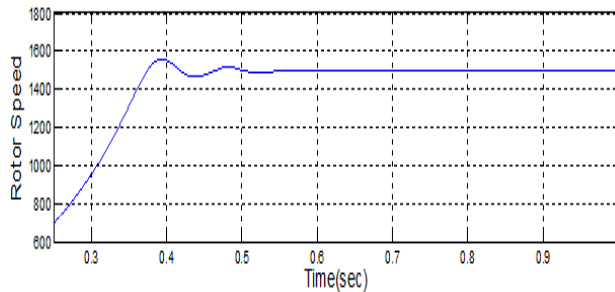


Fig.8 Rotor speed of 3-level inverter

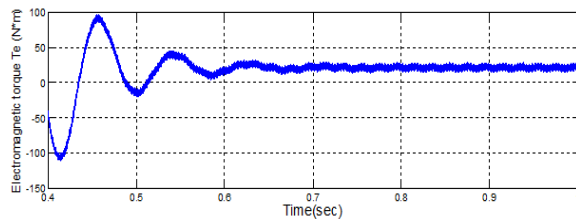


Fig.9 Electromagnetic torque of 3-level inverter

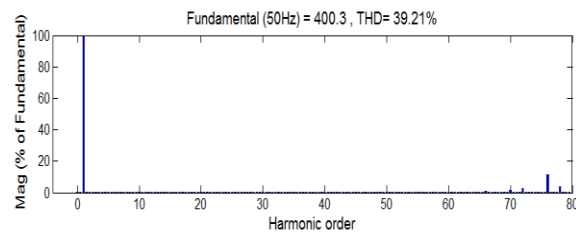


Fig.10 THD of 3-level inverter

B. Five- level inverter fed induction motor

Five-level inverter is modelled based on the theoretical concepts explained in chapter 3. Switching pattern produced for a five level inverter comprises of four triangular carrier and a reference sinusoidal waveform. Four pulses are generated which are given to the four switches of one leg of three level inverter. Similarly the pulses are generated for remaining phases. Modulating signal is phase shifted by 120 degrees. The corresponding line-line voltages and the performance parameter of

induction motor i.e. speed, torque (T_e), Rotor and stator currents, and total harmonic distortion are shown in fig.11-16.

1. Line voltages

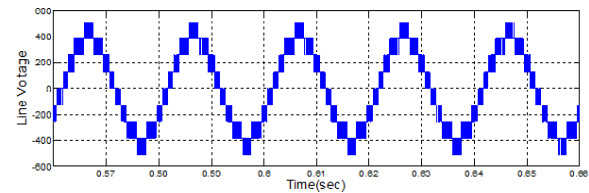


Fig.11 Five-level inverter line-line voltages

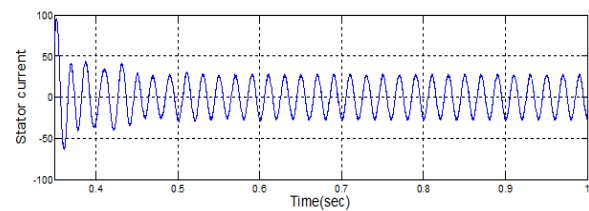


Fig.12 Stator current of 5-level inverter

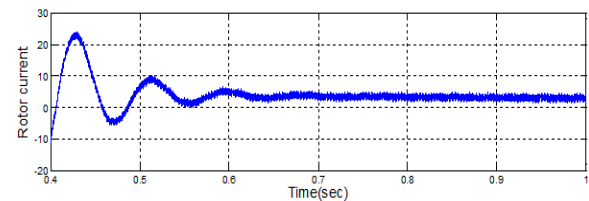


Fig.13 Rotor current of 5-level inverter

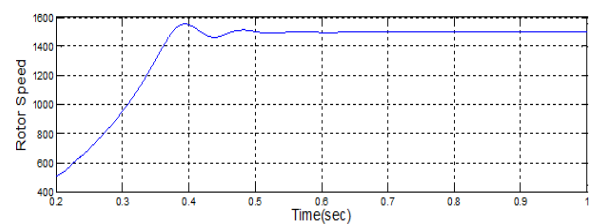


Fig.14 Rotor speed of 5-level inverter

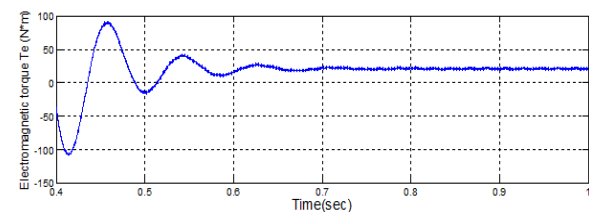


Fig.15 Electromagnetic torque of 5-level inverter

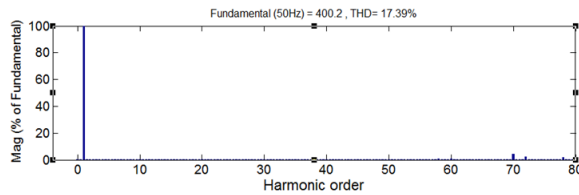


Fig.16 THD of 5-level inverter

C. Nine- level inverter fed induction motor
 Nine-level inverter is modelled based on the theoretical concepts explained in chapter 3. Switching pattern produced for a nine level inverter comprises of eight triangular carriers and a reference sinusoidal waveform. Eight pulses are generated which are given to the four switches of one leg of three level inverter. Similarly the pulses are generated for remaining phases. Modulating signal is phase shifted by 120 degrees.

The corresponding line-line voltages and the performance parameter of induction motor i.e. speed, torque (T_e), Rotor and stator currents, and total harmonic distortion are shown in fig .17-22.

1. Line voltages

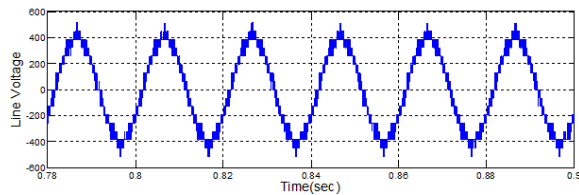


Fig.17 Nine-level inverter line-line voltages

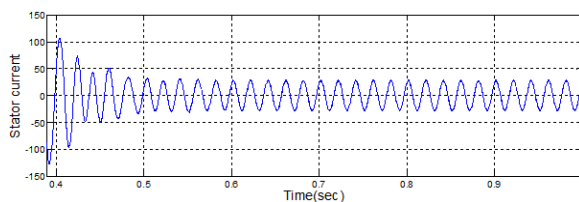


Fig.18 Stator current of 9-level inverter

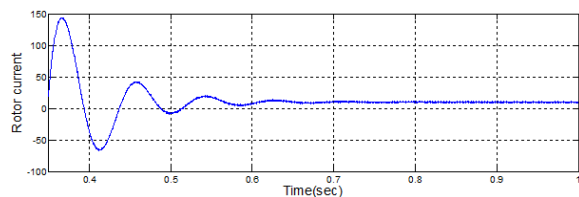


Fig.19 Rotor current of 9-level inverter

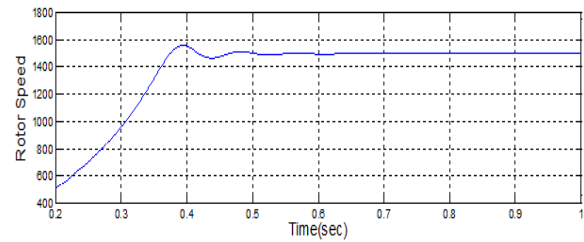


Fig.20 Rotor speed of 9-level inverter

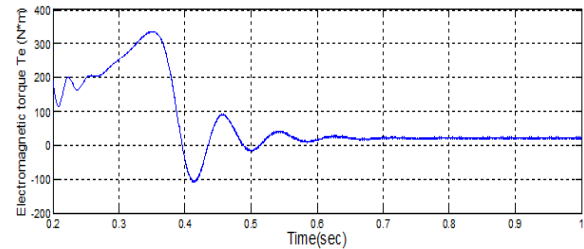


Fig.21 Electromagnetic torque of 9-level inverter

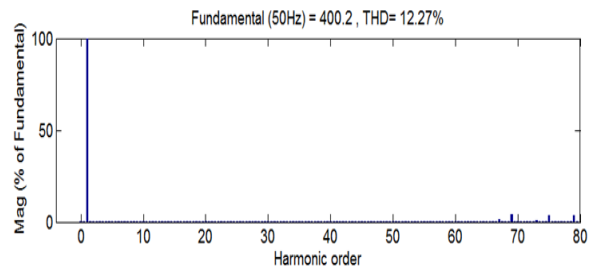


Fig.22 THD of 9-level inverter

7. Comparison of %THD

Table I shows the comparative analysis of THD between different levels of inverter. It is clear from the table that as the number of levels increases, the percentage of harmonics decreases.

Table. 1 % THD values of different level inverter

Parameters (Line voltages and Phase currents)	3-level (%THDVALUE S)	5-level (%THD VALUE S)	9-level (%THD VALUE S)
V_{ab}	39.21%	17.36%	12.26%
V_{bc}	39.20%	17.39%	12.27%
V_{ca}	39.20%	17.39%	12.27%
I_a	5.16%	2.25%	2.34%
I_b	5.18%	2.30%	2.34%
I_c	5.16%	2.25%	2.34%

8. Conclusion and Future Work

A comparative study on THD of output line-line voltage and current waveform of three-level, five-level and nine-level three-phase cascaded multi-level inverter has been presented in this paper as shown in Table I. using multicarrier sinusoidal pulse width modulation technique. It is observed that as the level of inverter increases, THD of line-line voltages and phase current decreases. Moreover there is improvement in the performance of induction motor with the increase in level of cascaded multi-level inverter. The sinusoidal pulse width modulation technique implemented in this paper also offers following advantages:-

- a) A low THD output waveform without any filter circuit is possible.
- b) Improved Switching loss problem.
- c) Electro-magnetic interference is minimised.

The future works include the fault-protection study for the cascaded multi-level inverter induction motor drives. Due to the excessive number of semiconductor devices and passive components, how to design a fault protection scheme to enhance the ride-through capability in various fault scenarios remains as an important challenge

References

- [1] Corzine, K.A., Familant, Y.L.: 'A new cascaded multi-level H-bridge drive', IEEE Trans. Power Electron., 2002, 17, pp. 125–131.
- [2] Teodorescu, R., Blaabjerg, F., Pedersen, J.K., Cengcelci, E., Enjeti, P.N.: 'Multilevel inverter by cascading industrial VSI', IEEE Trans. Ind. Electron., 2002, 49, pp. 832–838.
- [3] Lai, J.S., Peng, F.Z.: 'Multilevel converters – a new breed of converters', IEEE Trans. Ind. Appl., 1996, 32, pp. 509.
- [4] Kfir J. Dagan, Raul Rabinovici, Dmitry Baimel "analytical approach to the evaluation of harmonic content in multi-level inverters", IEEE Transactions on Industry Electronics, vol. 49, no. 4, Aug. 2010.

- [5] Rose, S. Flora Viji, and B. V. Manikandan. "Simulation and implementation of multilevel inverter based induction motor drive." In Control, Automation, Communication and Energy Conservation, 2009. INCACEC 2009. 2009 International Conference on, pp. 1-8. IEEE, 2009.
- [6] G.Durgasukumar, M.K.Pathak, "THD Reduction in Performance of Multi-Level Inverter fed Induction Motor Drive", IEEE Trans Indust~ Applications, vol. 32. No. 3, May 2012, pp. 509-517.
- [7] Jih-Sheng Lai, Fang Zheng Peng, "Multilevel Converters- A New Breed of Power Converters", IEEE Trans. On Industry Applications, vol. 32, no. 3, pp. 509-517, May/June 1996.
- [8] Fang Zheng Peng, Jih-Sheng Lai, et al, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation", IEEE Trans. on Industry Applications, vol. 32, no. 5, pp. 1130-1138, September/October 1996.
- [9] A. K. Ali Othman "Elimination of harmonics in multi-level inverter with non-equal DCsources using PSO".IEEE conf. proce EPEPEMC2008.
- [10] Gui-Jia Su; "Multilevel DC-link inverter," IEEE Transactions on Industry Applications, vol 41,no.3, pp.848-854, May-June 2005.
- [11] Najafi, E; Yatim, A.H.M.; "Design and Implementation of a New Multilevel Inverter Topology," IEEE Transaction on Industrial Electronics,vol.59,no.11,pp.4148-4154, 2012.
- [12] Wenxi Yao; Haibing Hu; Zhengyu Lu;, "Comparison of Space-Vector Modulation and Carrier-Based Modulation of Multilevel Inverter," IEEE Transaction on Power Electronics, vol23, no.1, pp.45-51, Jan.2008.



(India).

Naveen Kumar Verma was born in Begusarai (BIHAR), India, in 1988. He did his Bachelor of engineering in Electrical and Electronics stream from B.I.T.S, Bhopal (MP), India, in 2008 and pursuing his Master's degree in Electrical Engineering from Oriental College of Technology (OCT), Bhopal