

Implementation of 64-Point Reconfigurable FFT Processor for ASIP Architecture

B.S.Mahant¹, L.P.Thakare²

Abstract

In this paper a novel architecture of ASIP for a reconfigurable FFT is proposed. The proposed design implements a reconfigurable 64 points FFT processor for unsigned real numbers. By changing the value of integer constant we can design 2, 4, 8, 16, 32 and 64 point FFT which incorporates a high speed ASIP. In OFDMA system there is a need of alterable point FFT processor. Hence, the design meets the requirement of OFDMA system. DIF-FFT algorithm is implemented using VHDL language and Xilinx 9.1i is used for simulation results. The clock frequency is limited to 272.769 MHz for design stability and real time processing.

Keywords

FFT, DIF-FFT, OFDMA.

I. Introduction

FFT module is core part of OFDMA system as defined by IEEE Std 802.16-2005. The core module of OFDMA physical layer is the FFT module, which can be used in the FFT points are: 2048 points, 1024 points, 512 points, 128 points and 64 points. The design about variable point FFT processor is just based on FFT module in OFDMA system application. Hence this paper uses a reconfigurable FFT design for implementation of ASIP in OFDMA application for unsigned real number.

A variety of ASIP implementations have been presented for FFT algorithms. [3] used 2D FFT Algorithm to design the FFT Processor. According to the idea of two-dimensional Fourier algorithm, i.e. $N = 128$, $N_1 = 2$, $N_2 = 64$. From $128 = 2 * 64$. When achieve 128-point FFT, Firstly the data is arranged in 64 lines and 2 rows, secondly the input data will transform the 64 points FFT, then the result

multiplies twiddle factor, Thirdly, the result do 2 points FFT. For the classic Cooley-Tukey FFT (CT-FFT), different ASIP implementations have been presented.

In [4] instruction capable of calculating a whole butterfly operation is implemented and the computation resources are distributed into three execution stages to reduce the clock cycle. However, long pipelines consume more energy, and the speed-up from one integrated butterfly computation is still not enough to meet the high throughput requirement of the demanding IEEE 802.15.3a UWB communication standard. In [5] Hardware Extension is used for computations composed by four parallel butterfly units. A separate custom register file (CRF) is used to store all the intermediate data of the FFT computations in each epoch, and an on-chip ROM for the intra-epoch coefficients is used. An address changing logic (AC) is added in the decoder to give the right data address and coefficient address. It utilizes parallelism in the data path for performance in dissipation for the wide instruction length of 619 bits. The Xtensa ASIP design for FFT adds a set of, Therefore, after analyzing and comparison of various FFT algorithms, Decimation-In-Frequency FFT algorithm have been chosen. In order to ensure precision, the floating-point system is used in the design.

The paper presents a variable point FFT processor of a pipeline structure which is reconfigurable. The article is structured as follows. Fourier Transforms which is chosen in this design are illustrated in Section II. In Section III, the novel design of ASIP using reconfigurable FFT is proposed. In Section IV, the implementation and simulation is detailed. At last, the concise conclusions remark this paper.

II. Methodology

FFT is defined by the formula:

$$X_k = \sum_{n=0}^{N-1} x(n)W_N^{nk} \quad k=0,1,\dots,N-1 \quad (1)$$

Equation(1): N is Transform length, $W_N^{nk} = e^{-j2\pi/N}$ is Twiddle Factor.

B.S.Mahant, Electronics Engineering Department, G. H. Raisoni College of Engineering, Nagpur.

L.P.Thakare, Electronics Engineering Department, G. H. Raisoni College of Engineering, Nagpur.

The conventional method of FFT calculation involves N^2 complex multiplication and $N(N-1)$ complex additions.

The radix-2 Cooley-Tukey algorithm performs the same computation involving $(N/2)\log_2 N$ complex multiplication and $(N)\log_2 N$ complex additions. Algorithm is divided into frequency based (DIF) Fast Fourier Transform. The basic idea of these algorithms are that the N point FFT is divided into smaller and smaller parts until only two points FFT (Radix-2) is reached. Twiddle factor is considered as (-1) for all the butterfly computations.

III. Design of ASIP

Reconfigurable FFT module is core part of ASIP which can be used in various FFT points: 64 points, 32 points, 16 points, 8 points, 4 points, 2 points. The design is based on select module. It is based on input constant value given to the constant K to select the required points FFT: 64 points, 32 points, 16 points, 8 points, 4 points, 2 points. By defining this value the algorithm is compiled. After validity the architecture of the processor was modeled in VHDL language and functionally verified by Xilinx 9.1i software and timing simulations were obtained.

IV. Implementation and Simulation

A. RTL Schematics

The proposed design was synthesized at 3.66ns clock cycles. The RTL Block Diagrams for Reconfigurable FFT module for constant value of K: 64 is shown in Figure.1.

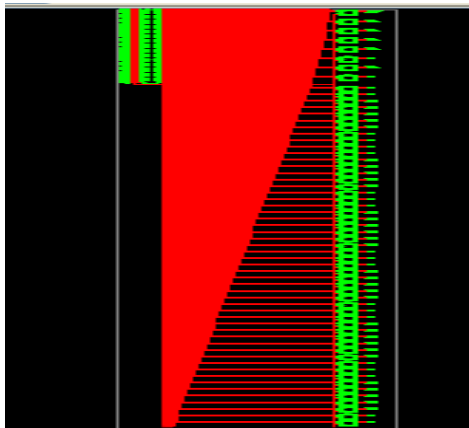


Figure.1: RTL View for 64 point FFT

B. Behavioral Simulation

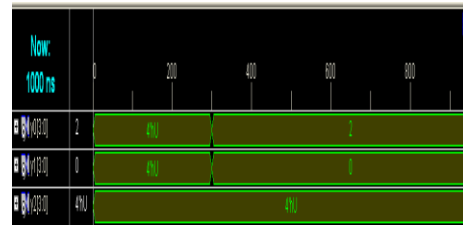


Figure.2: Simulation of 2 point FFT

When integer is 2 it gives 2 point FFT Output for input {1,1} comes to {2,0} is shown in Figure.2.

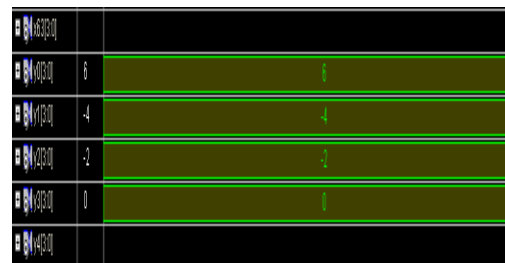


Figure.3: Simulation of 4 point FFT

Figure.3. shows that when integer is 4 it gives 4 points FFT.O/P for {0,1,2,3} comes to {6,-4,-2,0} assuming twiddle factor (-1) .

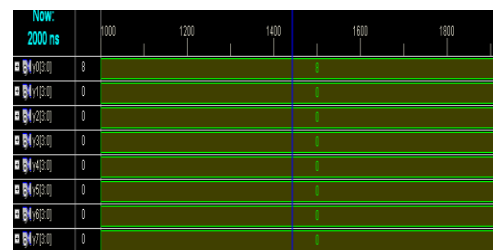


Figure.4: Simulation of 8 point FFT

Figure.4.shows the output for 8 points FFT For inputs {1,1,1,1,1,1,1,1} output is {8,0,0,0,0,0,0,0} with twiddle factor (-1)

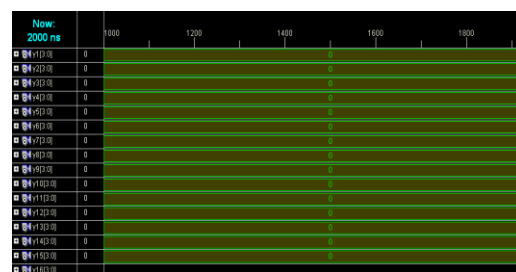


Figure.5: Simulation of 16 point FFT

Results in Figure.5 is for 16 points FFT with all inputs {1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1}



Figure.6: Simulation of 32 point FFT

For all the inputs considered as 1 Figure.6. gives the output with time cycle more than 1000nsec.

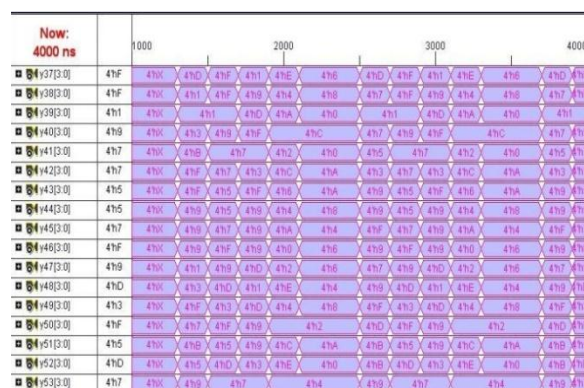


Figure.7: Simulation of 64 point FFT

With integer kept at 64 the design behaves as 64 points FFT. After this any value of integer say 128,256 and so on will give default results as in Figure.7.

V. Results

The FFT core in ASIP is computed with a speed of 272.769MHzs which is faster than 250MHzs [3] and 100MHzs [2].

VI. Conclusions

ASIP architecture for Reconfigurable FFT was proposed and implemented with high speed

performance. The successful completion of the design altered 2,4 ,8 ,16 ,32 and 64 points FFT. Computation, design for 64 points Reconfigurable FFT limited to 272.769MHzs clock frequency, with the overall timing design stability is obtained. Thedesign can be applied to real-time unsigned signal processing system, which completes the main computing modules in the OFDMA system.

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Miss.Bhagyashree S. Mahant
B.E., M.Tech G.H. Raisoni College of Engineering, Nagpur ISTE Member Designation:-Training and Placement Officer (Institute), I/C HOD, Electronics Dept.G.H. Raisoni Polytechnic, Nagpur.