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An Auto ranging Data Converter Implementation in FPGA

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Abstract

A novel project is being presented here for implementation an auto ranging analog to digital converter for biomedical applications completely inside an FPGA - i.e. an all-digital analog to digital (A/D) converter system. The only analog part is the auto ranging circuitry and an RC Integrator outside FPGA. The system outputs 24 bits and features a sigma delta ADC of 16 bits resolution, a range detection unit with 7 bits and a sign bit for polarity detection. The analog part of the modulator is done utilizing the LVDS transceiver in the FPGA making it a real digital one. The digital section of sigma delta ADC containing the decimation filter banks is done in a cascaded filter structure form including a CIC decimation filter, droop compensation and half-band filters. The top level module was coded using VHDL and the simulation was carried out with ModelSim and MATLAB.

Keywords

Autoranging ADC, Sigma Delta ADC, Digital filter section, 16 bit ADC.

I. Introduction

The sigma delta conversion technique has been in existence for many years, but recent technological advances now make the devices practical and their use is becoming widespread. The key feature of these converters is that they are the only low cost conversion method which provides both high dynamic range and flexibility in converting low bandwidth input signals. A sigma delta ADC consists of two parts –a sigma delta modulator and a digital filter section. The modulator consists of an analog filter and a coarse quantizer enclosed in a feedback loop. Together with the filter, the feedback loop attenuates the noise at low frequencies while emphasizing the high frequency noise.

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The oversampling sigma-delta modulation is a proven method to realize high and very high-resolution analog to digital converters. Because of the use of oversampling in sigma-delta modulators, the need arises for changing the sampling rate of signal, decreasing it to Nyquist rate in A/D-converters. Thus, the high resolution can be achieved by the decimation (sample reduction). Such sample reduction can be achieved employing high precision FIR filters, usually in cascaded structures The design of a decimation filter is proposed that employs three stage – one Cascaded Integration Comb filter (CIC) followed by two FIR filters. This approach eliminates the need for multiplication, requires a maximum clock frequency equal to the sampling frequency.

II. Top Level Design

The top level design in fig.1 is coded using VHDL [9]. It employs a shift register at the output to clock out the digital data serially so that this module can be attached to any serial communication protocol to send data. The auto ranging circuitry converts the analog data into the range of ADC and also outputs 7 bits representing the range of analog signal and 1 bit for sign. So altogether the unit outputs 8 bits along with the 16 bits from the adc to achieve 24 bits and the 24 bits imparts the end of conversion of one cycle and the data is moved to a shift register to clock out serially following assertion of a load signal.

III. System Design Considerations

Fig.2 shows the block diagram of a first order modulator. The analog input signal x (t) is sampled at the sampling frequency f, = 1/T. A quantizer with only two levels is employed so as to avoid the harmonic distortion generated by step-size mismatch in multi-bit quantizers. Out-of-band quantization noise in the modulator output is eliminated with a digital decimation filter that also re-samples the signal at the Nyquist rate. The power of the noise at the output of the filter is the sum of the in-band quantization noise together with in-band noise arising from other error sources, such as thermal noise or errors caused by jitter in the sampling time. An approximate expression for the quantization noise when the quantizer is modeled by an additive white-noise source is

$$S_B = \frac{\pi^4}{5}\frac{\Delta^2}{12}\frac{1}{M^2}, \qquad M \gg 1 \qquad \text{Eqn.1.}$$

The coefficient M is the over sampling ratio, defined as the ratio of the sampling frequency f, to the Nyquist rate. For every octave of oversampling, the in-band quantization noise is reduced by 15 dB.

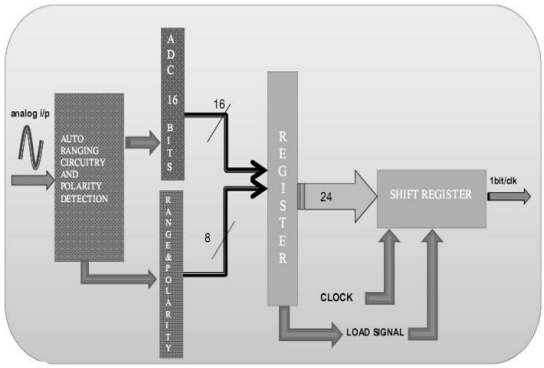

Fig 1: Block Diagram

Since the first order modulator can provide only limited resolution, we extend the noise shaping loop in the first order modulator to create a second order modulator.

IV. Second Order Sigma Delta Modulator

Second order sigma delta modulator consists of two integrators, 1-bit ADC, and 1-bit DAC. The power of the first integrator is the major consumption to the overall power dissipation in sigma delta modulator. For that reason, a substantial amount of power can be greatly saved by a suitable circuit design. The finite DC-gain, noise and distortion of the operation amplifier will be determined on the first integrator that will reduce the performance of the whole sigma delta modulator; since these errors will be added directly to the input signal, the advantages for this design can improve the noise in the sampling time to increase their solution of device, reduce the even harmonic and increase the input range.

It is clear that the SNR can be increased by increasing the over-sampling ratio in any order modulator. If over-sampling ratio increases, the modulator will be operated in higher speed and consumed more power. So, further power saving can be achieved by using relatively low over-sampling ratios (OSR=fs/2fin). The modulator is followed by a digital down sampling section, which we call the decimation filter stages.

V. Digital Decimation Filters

Multipliers represent most of the hardware used to implement a filter; as a result, multipliers contribute to most of the power dissipated in a filter. The comb filters do not require multipliers; therefore, they have been cascaded in the beginning of the Comb-FIR chain. Comb filters have a drawback of poor stop band attenuation. The 4-stage comb filter we are using provides a stop band attenuation of -58dB.

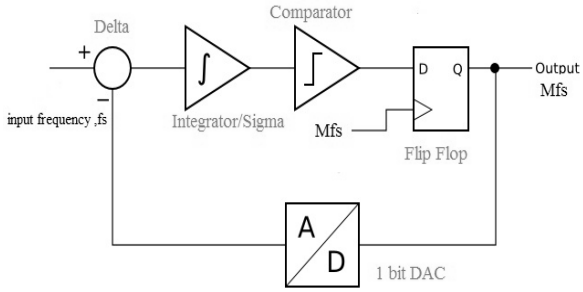

Fig 2: First Order Sigma Delta Modulator

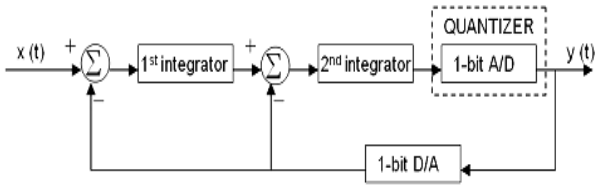

Fig 3: Second Order Sigma Delta Modulator

The final output of the decimationfilter has a16-bit accuracy. This accuracy is supportedby 5dB/bit stop band attenuation. Comb filters aredescribed by the following equation:

$$H(z) = (1/M)^S . (1 - z^{-M})^S . (1/1-z^{-1})^S \qquad \text{Eqn.2}$$

Where *s* represents the number of stages cascaded, and M represents the decimation factor. Eqn.2. is further divided into an integrator represented by $(1/1-z^{-1})$ anda differentiator represented by $(1-z^{-1})$. We use the architecture of the comb filter, which consists of four integrators, a divide by 256 down sampler and four differentiators, as shown in Fig. 4.

Since the Cascaded Integral Comb[7] filters have a finite gain of the exponential power product of differential delay and oversampling ratio, and a definite droop in pass band we have to compensate for both while designing the digital filter stages. For compensating the finite DC gain of CIC filter we have to multiply the filter with its inverse DC gain

and there by compensating the dc gain and normalizing the filter. Now to compensate for the droop in the pass band we have to use a filter which has exactly the reverse characteristics of CIC filter in the pass band. Since the CIC filters have a sinc type response we will need a filter which is having an inverse sinc characteristics. Cascading this filter with the original eliminates the droop in pass band problem. This will be followed by two FIR filters having a decimation factor of two each. The last stage is a half band filter. It's a FIR filter with the even co-efficient zero and is symmetric. Since the filter is symmetric the co-efficient calculation arithmetic is largely reduced. Here the FIR algorithm chosen is a derived version of Parks-McClellan algorithm –generalized remez algorithm. The advantage of choosing the remez algorithm is that along with all the well-spoken advantages of FIR filters, it allows us to choose the ratio of allowable ripple in pass band to allowable ripple in stop band.
The overall filter response will have stop band attenuation much higher than 60 dB.

VI. Taking Advantage of LVDS Input Buffers

Now, with the most recent FPGA families supporting the Low-Voltage Differential Signaling

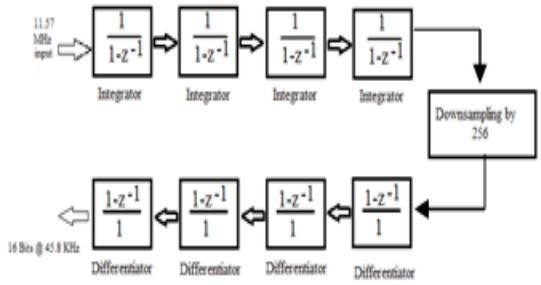

Fig 4: The four stage comb filter structure

(LVDS) standard, the implementation of ADCs in an FPGA becomes feasible. [1]

LVDS is a low swing, differential signaling technology which allows single channel data transmission at up to hundreds of megabits per second. It is mainly used for digital communication between different devices at very high speeds. Instead of one output pin and one input pin as in usual interfacing schemes, differential signaling works with two complementary signals, allowing for a better noise immunity and lower voltage levels.

By taking advantage of this LVDS comparator, Analog to Digital converter can easily be implemented within the FPGA with additional analog components used. Sigma Delta modulator topology can make use of the FPGA LVDS comparator to perform integration function by using an external RC network. Among the many advantages of this modulator, the most important is that they are easilyintegrated in a digital chip.

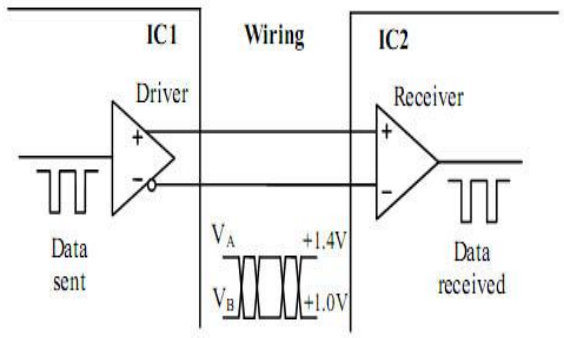

Fig 5: Simplified Diagram of LVDS Transceiver

Fig.6. shows the implementation diagram of the second order sigma delta modulator inside the FPGA. Two LVDS comparators have been used to create a second order version of sigma delta modulator accounting for the high resolution of 16 bits. The digital filtering, which consists of the cascaded filter stages will be done using the programmable resources available in the FPGA.

VII. Simulation Results

The digital filters were modelled using MATLAB as shown in Fig.7. and the simulation result of the output of the digital filter stages is shown in Fig. 8. It can be noted from the output of the filter stages that the stop band attenuation is much greater than 60 dB which is at par with the communication standards ofDDC (Digital Down Converters).

The FPGA used for the setup is an Altera Development board containing Stratix II FPGA. Stratix II is one of the fastest FPGAs available in the industry in its contemperory 90 nm technology.With Quartus II software as a platform for simulation and programming the FPGA, the result obtained here shows how the oversample bit stream is obtained using the LVDS comparator in the FPGA.

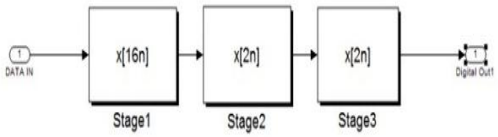

Fig 7: Block Diagram Filter Stages

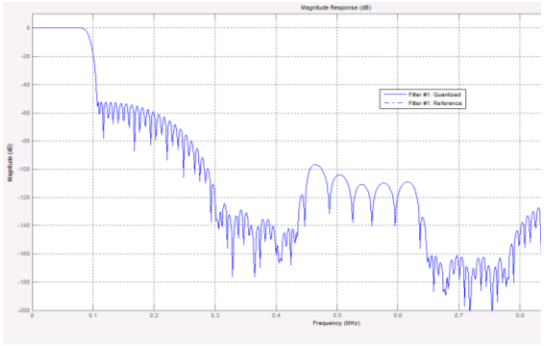

Fig 8: Simulated Output of Decimation Section

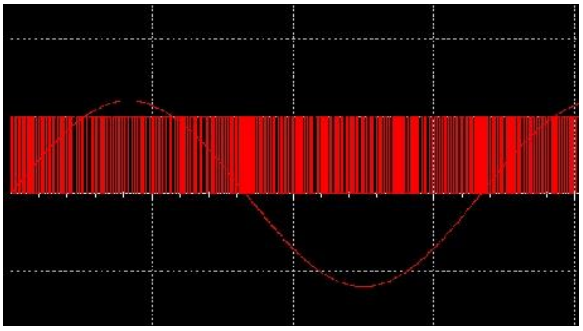

Fig. 9: Show the simulation result of the second order modulator.

The frequency spectrum of the second order modulator simulated using MATLAB is shown in Fig. 10.

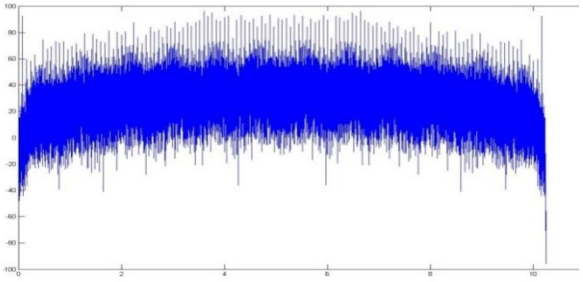

Fig.10: Spectrum of Second Order Modulator

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Sreekumari B is a senior scientist working Power electronics group of CDAC. She is having an experience of 29 years in areas of Design and development of embedded controllers and power electronic controllers, Automatic test equipments, remotely operated mobile platforms, solar inverters, Medical Electrical Safety Analyzers.

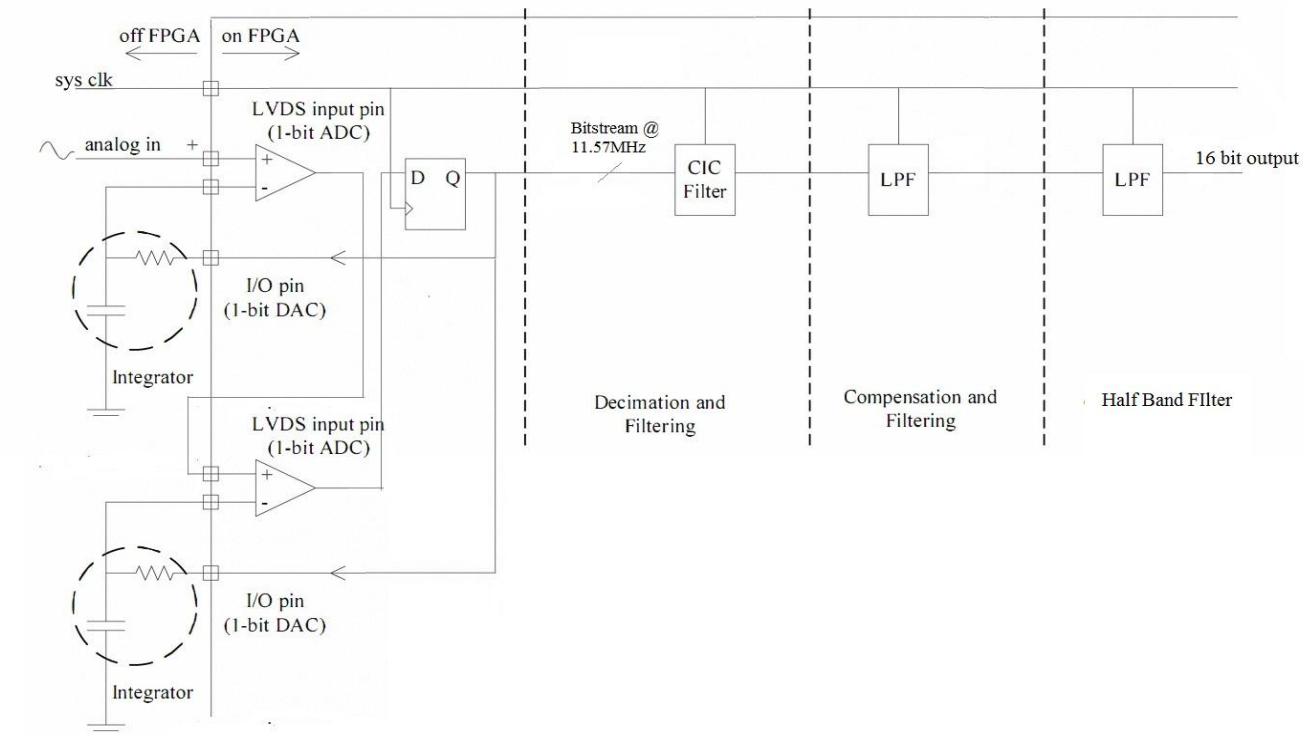

Fig.6: Implementation diagram of S-D ADC using LVDS