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Implementation of MAC by using Modified Vedic Multiplier

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Abstract

Multiplier Accumulator Unit (MAC) is a part of Digital Signal Processors. The speed of MAC depends on the speed of multiplier. So by using an efficient Vedic multiplier which excels in terms of speed, power and area, the performance of MAC can be increased. For this fast method of multiplication based on ancient Indian Vedic mathematics is proposed in this paper. Among various method of multiplication in Vedic mathematics, Urdhva Tiryagbhyam is used and the multiplication is for 32 X 32 bits. Urdhva Tiryagbhyam is a general multiplication formula applicable to all cases of multiplication. Adder used is Carry Look Ahead adder. The proposed design shows improvement over carry save adder.

Keywords

MAC, Vedic multiplier, VHDL, Carry Look Ahead adder.

1. Introduction

Digital multipliers are the core components of all Digital signal processors. The speed of DSP is largely determined by the speed of its multipliers. Multiply Accumulate (MAC) operation is a commonly used operation in various Digital Signal Processing Applications. Use of a Digital Signal processor can significantly increase the performance of a MAC. Normally a multiply accumulate unit consists of a multiplier along with an accumulator which stores previous multiplication products. Since system performance widely depends on time needed to execute the instruction and multiplication being the most time consuming any improvement to multiplication will inherently improve the system performance. Multiplication can be implemented using several algorithms such as array, Booth, carry save, Modified Booth algorithm and Wallace tree in array multiplier multiplication of two numbers can be obtained with one micro operation. It is a fast method of multiplication since the only delay is time for the signals to propagate through the gates. But it requires larger number of gates and so it is less economical.

In the carry save method, bits are processed one by one to supply a carry signal to an adder located at a one bit higher position. The limitation of this method is that its execution time depends upon the number of bits of the multiplier. In the Wallace tree method, the circuit layout is not easy although the speed of the operation is high. The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums. But the drawback is power consumption [1].

A new algorithm is developed that uses Vedic mathematics. The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics. The Vedic algorithm is applicable to arithmetic, trigonometric, plain and spherical geometry, calculus. The whole of Vedic mathematics is based on 16 sutras. Here we use Urdhva Tiryagbhyam of Vedic mathematics. This sutra was traditionally used in ancient for the multiplication of two decimal numbers in relatively less time [2]. The architecture of urdhva tiryagbhyam is explained that any NxN multiplication can be efficiently implemented by breaking it into smaller numbers of size (N/2=n) and these smaller numbers can again broken into smaller numbers (n/2) till we reach multiplicand size of (2 x2). Thus simplifying the whole multiplication process. This work present a systematic design methodology for fast and area efficient digital multiplier based on Vedic mathematics and then a MAC unit has been made which uses this multiplier [5].

2. The Proposed MAC Unit

The multiply accumulate unit computes the product of two numbers and adds that product to an accumulator. The MAC unit consists of a multiplier followed by an adder and an accumulator register which stores the result.

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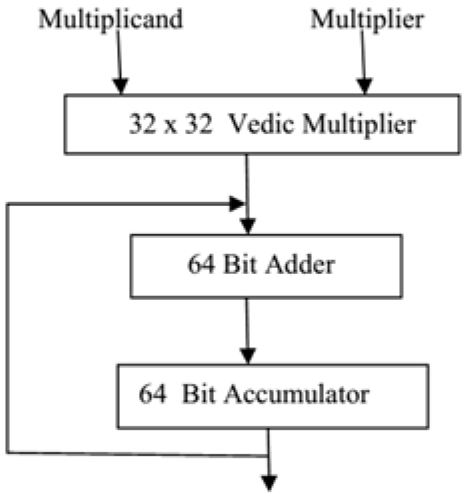


Fig 1: Architecture of MAC

The architecture of the designed MAC unit is shown in the figure 1. The two input 32 bit operand to the MAC unit are A [31:0] and B [31:0].The 32 bit output from MAC unit is q[63:0]. The proposed design uses one 32x32 Vedic multiplier using Urdhva Tiryagbhyam algorithm. 64 bit accumulator using carry look ahead adder and one 32 bit register. Vedic multiplier design can increase MAC unit design speed.

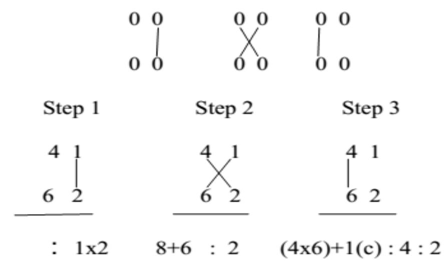
3. Vedic Mathematics Principle

Vedic mathematics is the name given to the ancient system of mathematics, which was discovered between 1911 and 1918 by Sri Bharati Krishna Tirthaji. The word "Vedic" is derived from the word "Veda" which means the store house of all knowledge [3]. The Vedic mathematics is based on 16 sutras which deal with various branches of mathematics. These sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The possible multiplier architecture of Vedic mathematics to be implemented on DSP applications is Urdhva Tiryagbhyam. Traditional Indian mathematicians used this sutra to do multiplication of two decimal numbers in less time. It multiplies the number in the vertical and crosswise fashion. It is applicable to all cases of multiplication [2].

3.1 Urdhva tiryagbhyam sutra

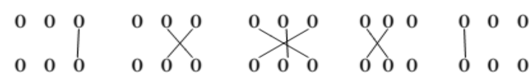
Urdhva Tiryagbhyam is the general multiplication formula applicable to all cases of multiplication. 'Urdhva' and 'Tiryagbhyam'words are derived from Sanskrit literature. It literally means "vertical and crosswise". Multilpication of two and three digit numbers with this method as follows [3].
Multiplication of 2, two digit numbers as shown:

General rule for 2x2 multiplication



The product is 2542.

General rule for 3x3 multiplication



Similarly for any number of digits the multiplication technique of ancient Indian Vedic mathematics can be used.

4. Hardware Realisation

The hardware realization of the two bit number using the concept of the Urdhva- Tiryagbhyam sutra of the ancient Indian Vedic mathematics is shown in Fig 2.

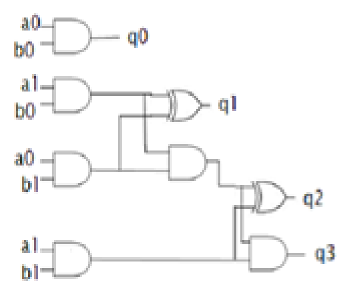


Fig 2: Hardware Realization of 2*2 Hardware

4.1 4x4 Multiplier

The 4x4 multiplier is made by using 4, 2x2 multiplier blocks. For the output to be a 8 bit one the multiplicands should be inherently 4 bit(n=4). The input is broken into small units of size n/2=2. The newly formed units of 2 bits are given as input to 2x2 multiplier blocks and the result produced is 4 bits [4].

The output of the 2x2 multiplier is loaded to the addition tree for further operation. The block diagram is shown in Fig 3. Let the two numbers A and B of four bit each and and as per the sutra they will be divided into two, two bit numbers to reduce complexity. It will leads to high efficiency multiplier architecture.

A= a3 a2 a1 a0 (multiplicand)
B= b3 b2 b1 b0 (multiplier)

These four bit input is divided into two bit numbers.

A1= a3 a2   A0= a1 a0 &
B1= b3 b2   B0= b1 b0

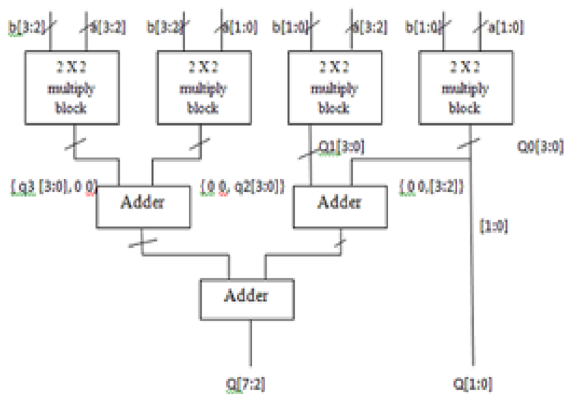


Fig 3: 4*4 Multiply Block

4.2 8x8 Multiplier

The 8x8 multiplier is made by using 4, 4x4 multiplier blocks. Here the multiplicands are of bit size (n=8) and the output is of bit size 16. The input is broken into small units of size n/2= 4. The newly formed units of 4 bits are given as the input of 4x4 multiplier block,where again these units is divided into even smaller units of size n/4=2 and fed to 2x2 multiply block. The output obtained from output of 4x4 bit multiply block which is of 8 bits are sent for addition to an addition tree. The block diagram is shown in Fig 4.

Let the two numbers A and B
A= a7 a6 a5 a4 a3 a2 a1 a0
B= b7 b6 b5 b4 b3 b2 b1 b0
The input is divided into small bits of four bits.

A1= a7 a6 a5 a4   A0=a3 a2 a1 a0 &
B1= b7 b6 b5 b4   B0= b3 b2 b1 b0

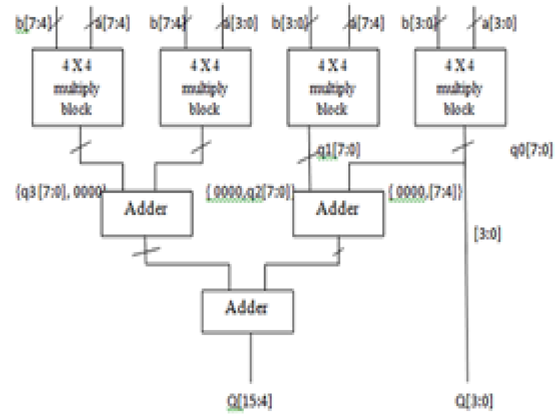


Fig 4: 8*8 Multiply Block

4.3 16x16 Multiplier

The 16x16 bit multiplier is made by using 4,8x8 multiplier blocks. Here the multiplicand are of size (n=16) and the result obtained is 32 bit size. The input is broken into small unit of size n/2=8. These newly formed units are given as input to 8x8 multiplier blocks. Again the new units are broken into even smaller units of size n/4=4 and fed to 4x4 multiply block. The newly formed 4x4 bit unit is again divided in half to get unit of size 2, which is fed to a 2x2x multiply block. The result produced from output of 8x8 bit multiply block which is of 16 bits are sent for addition to an addition tree.

Let the two numbers are
A = a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0
B = b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0

The input is divided into small units

A1 = a15 a14 a13 a12 a11 a10 a9 a8
A0= a7 a6 a5 a4 a3 a2 a1 a0 &

B1= b15 b14 b13 b12 b11 b10 b9 b8
B0= b7 b6 b5 b4 b3 b2 b1 b0

Again it is divided into small unit of size 4

A1a= a15 a14 a13 a12   A1b= a11 a10 a9 a8
A0a= a7 a6 a5 a4   A0b= a3 a2 a1 a0

B1a = b15 b14 b13 b12   B1b = b11 b10 b9 b8
B0a = b7 b6 b5 b4   B0b = b3 b2 b1 b0

The block diagram is shown in Fig 5.

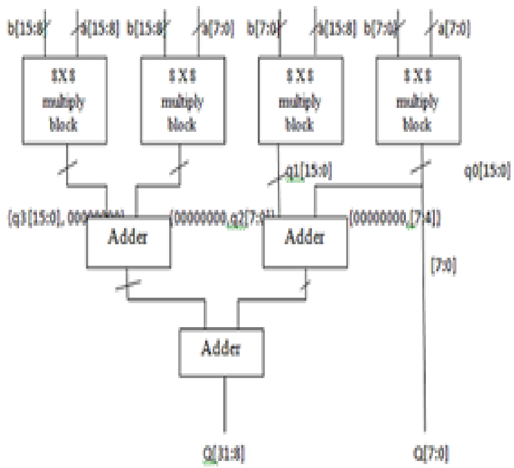


Fig 5: 16*16 Multiply Block

5. Simulation Result

It is observed that for 16x16 Vedic multiplier the delay obtained is 21.4ns. Model sim is used for simulation and synthesis of the Vedic multiplier is carried out using Xilinx ISE 10.1. Hence the proposed multiplier architecture is found to be most efficient in terms of speed. Fig 6 displays the simulation result of 16x16 Vedic multiplier.

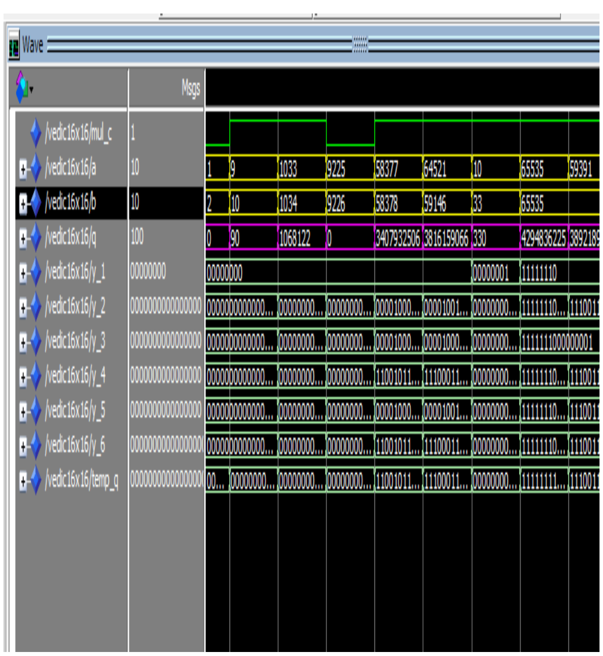


Fig 6: Simulation Results

Table 1 shows the synthesis result of 16x16.The delay of 16x16 Vedic multiplier is 21.4ns with nearly 8% device utilization.(number of slices: 508 out of 704) and number of 4 input LUTs: 98 out of 1408(6%). The number of bonded IOBs: 28 out of 108(25%).

Table 1: Synthesis Result

Algorithm	Proposed 16 bit multiplier
Delay(ns)	21.4 ns
Number of Slices	58 out of 704 (8 %)
Number of 4 Input LUTs	98 out of 1408 (6 %)
Number of bounded IOBs	28 out of 108 (25 %)

6. Conclusion and Future Work

Urdhva Tiryagbhyam Sutra is highly efficient algorithm for multiplication. The design of 16x16 bit Vedic multiplier has been realized on Spartan 3A and Sparta n 3AN. The computation delay obtained for 16x16 Vedic multiplier is 21.4ns and the device utilization is 8%. which shows improvement in performance.

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