International Journal of Advanced Computer Research (ISSN (print): 2249-7277 ISSN (online): 2277-7970)
Volume-4 Number-1 Issue-14 March-2014

The Effect of Radiations on the Structural and Electrical Properties of Device Technologies: Comparison and Trends

C P Jain

Abstract

The effects of radiation on the structural and electrical properties of electronic devices are complex in nature and have changed much during decades of device evolution. These effects are mainly because of radiation induced charge build-up in oxide and interfacial regions. This paper presents a details of these radiation induced effects, their dependencies, and the change in structural properties and electrical characterises of different devices before and after irradiation are measured and comparison results are reported. The Radiation hardens characteristics of different devices are measured in rad/s.

Keywords

CMOS Circuits, MOS Devices, HBTs, HEMTs, Bipolar Devices, Radiation Effects, Radiation Hardening.

1. Introduction

In this paper, we mainly focus on to study the device and circuit under radiation environment or harden against the radiation and for bipolar process; for years, Si BJT, CMOS has been widely used all over in the semiconductor and integrated circuit technologies [1],[2],[3]. A massive research that has been done into silicon technology (MOS, CMOS etc) over the many years has resulted in incredibly cheap, reliable, and simple manufacturing and design processes [3]. The mysterious world of the III-V transistor and other band gap-engineered technologies occupies only a small slice of the overall semiconductor pie due to the expensive cost and low-yield typical of these advanced platforms [2]. These technologies are used only for those applications where we require the highest speed, lowest-noise, and highest gain [2].

Manuscript received February 07, 2014.
C. P. Jain, Department of Electronics, Banasthali University, Banasthali, Rajasthan, India-304022.

Clearly, a space qualified IC technology must show sufficient radiation tolerance to support high speed circuit applications as well possess total dose tolerance. SiGe & III-V HBT, HEMTs technology has generated considerable interest in the space community due to its robustness to total ionizing dose radiation (TID) without any additional hardening. But, recently it has found that high speed HBTs digital logic circuits were vulnerable to SEU [4]. Hence it is important to study the radiation effect on HBTs as well as CMOS and MOS devices. To understand these effects in these devices, we use calibrated two dimensional (2-D) device simulations to assess the characteristics of devices with and without radiations.

2. Simulation Details

In this simulation, we define radiation dose as the amount of energy exposed on the material used and the unit of stimulated radiation dose are given in Rads. As the loss of energy is depended on type of material so that it is added onto the unit. A given radiation dose is used in considering a mass of material. The expression dose rate is employed to point out the dose per unit time (e.g. Gy/min or Rad/min) that a device will experience at a position from a radiation source.

In Technology Computer Aided Device (TCAD) tool, Devices simulation is divided into two different models that are calculated simultaneously at each DC bias point or transient time step.

l. Optical ray trace using real component of refractive index to calculate the optical intensity at each grid point.
2. Absorption or photo-generation model using the imaginary component of refractive index to calculate a new carrier concentration at each grid point.
Here we define the photo-generation rate in a C-INTERPRETER function written into a text file that can be supplied to the program. The file returns a time and position dependent photo-generation rate to the program. This returned value is multiplied at every node point defined during mesh initialization.

The X. ORIGIN, Y. ORIGIN and X. END, Y. END parameters set the coordinates of the starting and the last point of the line segment. The default values correspond to the top left and bottom left corners of the device considered .The Standard beam input syntax allows specification of plane waves with Gaussian or flat-top (top-hat) irradiance profiles.In this simulation, we have assumed that the radiation on the device has created a uniform Photo-generation rate of different dose rate vary from 1E10 to 25E30 on devices.

3. Device Characterization

3.1 Bipolar Technology

From simulation results in figure 1 & 2, it is seen that as we increase the radiation dose, the drain current increases. These trapped charges produce new interface states at the frontier SiO_2-Si interface that also decreases minority carrier lifetime and increases the junction leakage current. The impact of oxide trapped charges on bipolar devices is much smaller than for MOSFETs because the oxide is not an active part and the surface doping is much greater for bipolar transistors than for MOSFETs. Both bulk and interface defects decrease the overall gain and increases the leakage current. The major effects of radiation on bipolar transistors are a gain loss and an increase of leakage current. The degradations are higher for power bipolar transistors, especially at low currents. The damages that produced from a high dose rate exposure of a bipolar transistor are smaller to the ones that can be found with a low dose rate [3].
In this simulation, the Ic verse V_{ce} characteristic is plotted for different values of base current of the silicon BJT using Gummel model, the syntax for the I_c/V_{ce} simulation is described in considering above NPN structure. The key point is the use of current boundaries conditions on the base contact as defined by contact name = base current. This allows constant base current to be forced while V_{ce} is ramped. The family of I_c/V_{ce} curve can be overlaid in plot.

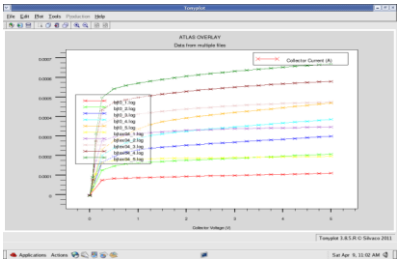

Figure 1: Overlay results of I_d/V_d for dose 7e12

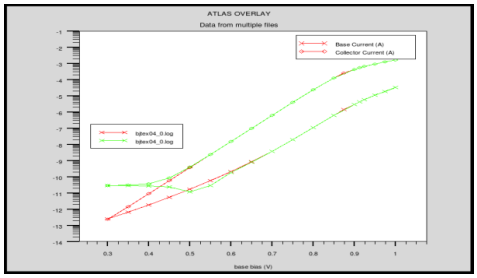

Figure 2: Result for dose2E20

As shown in figure the bipolar devices are subject to enhanced low dose rate sensitivity effects. These depend on the design of the device. Transistors show the current gain degradation and the low dose rate effect is higher. Displacement damage can be important in some cases and single event gate rupture has been observed.

3.2 The SiGe HBT Technology

The study of radiation effects on SiGe technology can be divided into two main topics. Total ionizing dose (TID) and single event effects (SEE). TID effects are those caused by long-term exposure to radiation that slowly ionizes the oxides within a device and usually appears as increased base leakage current.

Figure 3 to figure 5 shows the Gummel plot characteristics of a SiGe HBT (which has not been radiation hardened in any way) both before and after exposure.

The majority of this is similar to Silicon bipolar Gummel plot in BJT section, this description will focus on the specific SiGe syntax.
In this model, we specify common models for Si and SiGe regions, but this is not essential. The material parameter of the model statement can be used to set separate model for each material.
The electrical part of this file is same as the silicon file above.

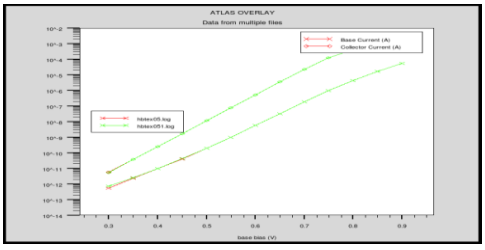

Figure 3: Result for dose 1E18

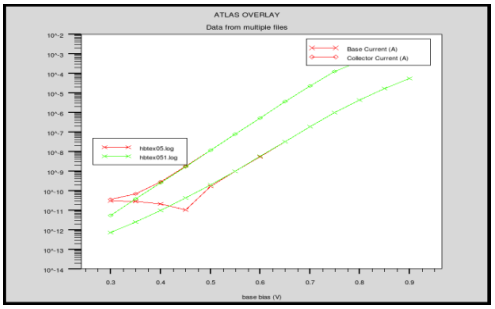

Figure 4: Result for dose 2E20

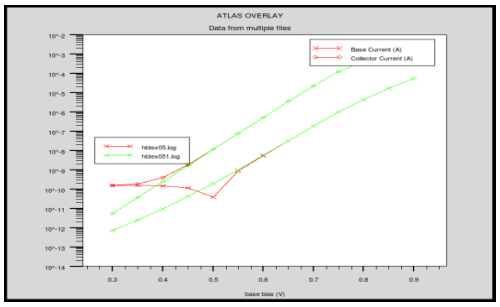

Figure 5: Result for dose 10E20

The data, shown in Figures, indicates little difference between the two at low doses, but a larger variation for higher dose rate.Such devices are therefore competitors for GaAs devices for use in satellite communications systems. Implementing SiGe in BiCMOS opens the way for mixed mode analogue-digital applications. In addition, the SiGe HBT can be optimized for cryogenic applications.

3.3 GaAs /AlGaAs HBT Technology

In this simulation we take the simulation of an AlGaAs/GaAs HBT to extract I_c and I_b verse V_{be} and plot the bipolar gain. The majority is similar to the Silicon bipolar Gunmmel plot. Here we focus on specific AlGa and AlGaAs syntax.The low field motilities for the AlGaAs region is set in the material statement. Keep in mind that the concentration dependent mobility model 'conmob' can be applied to GaAS so two model statement are used to defined the model used in all region and then just the GaAs region.

The model statements are used to specify the following set of models: field dependent mobility, SRH and optical recombination. Optical recombination (also known as band to band recombination) is important effect in III-V devices. The electrical simulation is same as in silicon BJT.

From figure 6 to figure 8, it is seen that to illustrate GaAs field effect transistor (FET) does not have any oxide that can trap charges. Little threshold voltage shift resulting from charge trapping is experienced. Radiation creates defect centres in the emitter and base materials. These two effects increase the base current and lead to a small decrease of current gain [5].

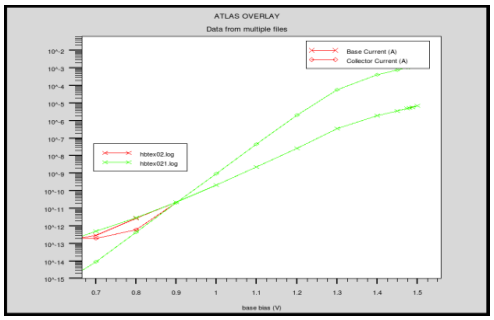

Figure 6: Result for dose 1E18

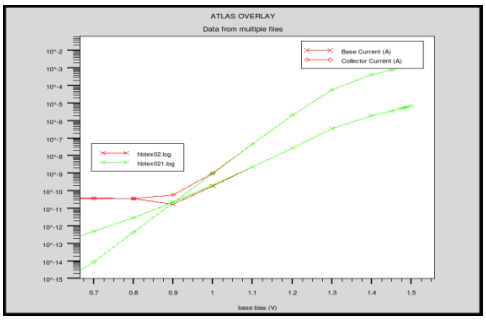

Figure 7: Result for dose 2E20

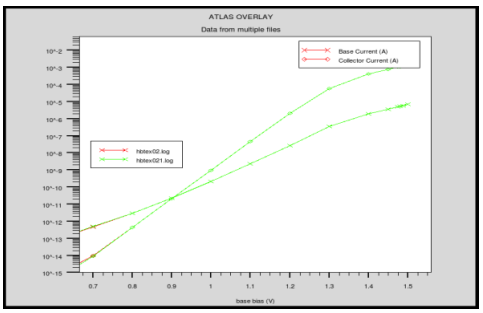

Figure 8: Result for dose 2E15

Since no dielectric layers are used the devices show some radiation tolerance - up to several hundred Mrad (GaAs), which is two orders of magnitude higher than for equivalent Si-based technologies. In general GaAs technology is very susceptible to SEU.

As for GaAs devices, displacement damage is the only radiation concern.

3.4 InP/InGaAs HBT Technology

An HBT structure based on the InGaAs-InP material created. The structure is then passed to ATLUS for electrical stimulation. The simulation is first performed to obtain the Gummel plot by biasing simultaneously the base and collector with respect to the emitter up to 12 V. The simulated ID . $V_{G\ and}$ I_B-V_G characteristics of an InP HBT transistor with different levels of hot carrier damage [6]. As expected the threshold voltage increases as a result of oxide interface charge. As a result changes in drain current and base current by using different radiation doses applies.

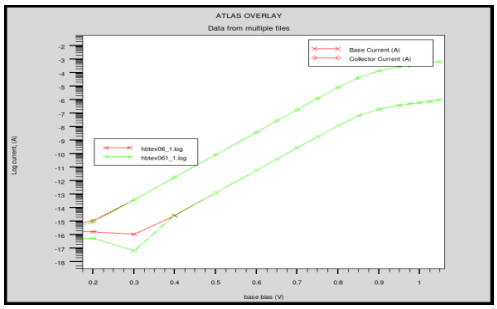

Figure 9: Result for dose 1E15

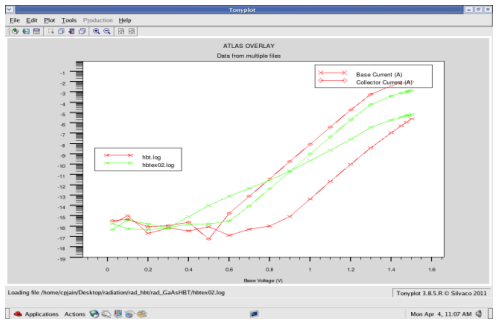

Figure 10: Results of dose 2*10E6

This material shows promise for high speed applications but is in the early stages of development. Displacement damage is probably the key issue.

3.5 High Electron Mobility Transistor (HEMT) Technology

High electron-mobility transistors (HEMTs) are promising candidates for future RF and mixed-signal circuit applications. It gives high performance at low cost by offering compatibility with standard CMOS logic processes. Their mobility advantage at low drain voltage and current levels compared to conventional CMOS makes them very attractive candidates for high speed and low power applications. Currently, impressive levels of device performance have been achieved [7].

A commonly used material combination is GaAs with AlGaAs however; there is wide variation, dependent on the application of the device. The device is created same as the previous structures. After the initial solution is obtained, the gate voltage is set to 0, the structure under zero bias is displayed using plot, and the I_d- V_{ds} characteristic is calculated. The drain voltage is first ramped up to 0.3 V. the solution are obtain using the combined Gummel-Newton algorithm specified in the method gummel newton statement. The algorithm implies that if solution does not converge in the course of gummel iteration, the program will automatically switch over to the newton algorithm. Next in the drain voltage is ramped up to 3V. This part of simulation is performed using the Newton method. Simulation of the I_d- V_{gs} characteristic is performed next. At the first stage the solution for V_{gs} = 0.9 V and V_{ds} = 0.5V is obtained, next the voltage is ramped up to 0.6V with the step of 0.1V. In this simulation we consider I_d-V_{ds} and I_d-V_{gs} calculation in a single quantum-well ALGaAs/GaAs HEMT structure.

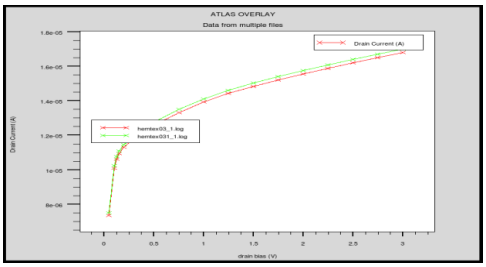

Figure 11: Result of dose 1E15

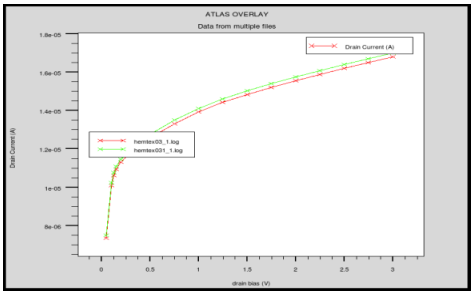

Figure 12: Result of dose 2E20

3.6 Complementary Metal Oxide Semiconductor (CMOS)

CMOS-Bulk Devices (IC's) experience "latch up" due to a parasitic four-layer PNPN path, inherent in most unhardened devices. These parasitic four-layer devices acts like a Silicon Control Rectifier (SCR), which once latched cannot be turned off without shutting off the power. If the CMOS-bulk process creates parasitic SCR's or PNPN structures, the excessive charge may cause a Latch up, leading to a SEL, which can sometimes lead to the destruction of the device.

Another potentially catastrophic SEE phenomenon called "Snapback" exhibits many of the characteristics of latch up and can occur in single MOS transistors structure. A single high energy particle may trigger snapback if the field across the drain region is sufficiently high. Snapback is due to the prospect of a parasitic bipolar transistor existing between the drain and source region of a MOS transistor which amplifies avalanche current that results from the transversal of the heavy ion cosmic ray particle and generate a very high current between the drain and source region of the transistor, with subsequent localized heating.

As shown in the basic CMOS inverter circuit after irradiation, the most important changes are the switch point, the decreased output rail voltage, and the increased leakage current. If radiation becomes strong enough, proper switching operation may fail [8].

The uniform photo-generation rate of 1 x 10^{25} s^{-1} cm^{-3} is defined using C-INTERPETER function as shown on the Fig. 3 & 4.

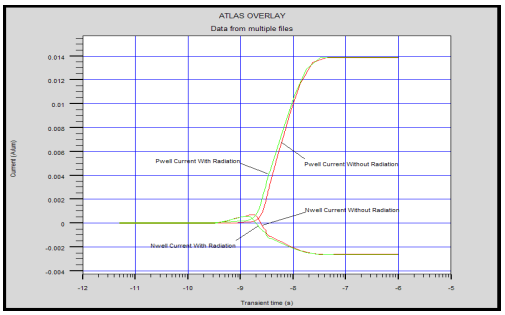

Figure 13: Transient Pwell & Nwell current Simulation of CMOS with and without Radiation

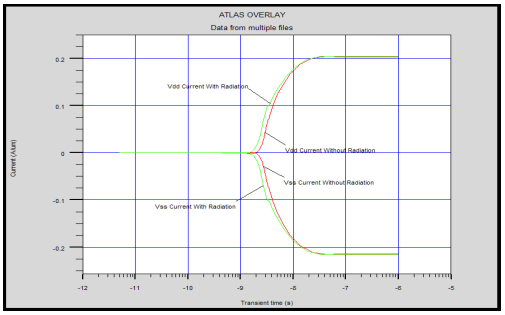

Figure 14: Transient V_{dd} & V_{ss} current Simulation of CMOS Device with and without Radiation

3.7 Metal Oxide Semiconductor (NMOS) devices

From figure 15 to 16 it has shown the illustration of the gate voltage and drain voltage dependence of the effects of ionization, in an n-channel MOS device irradiated with a high dose rate, the threshold voltage shift is due to positive trapped charges. The n-channel threshold voltage shift is plotted as a function of I_d/V_{gs} of radiation doses. As the radiation dose increases, the threshold voltage of NMOS devices will decrease [9].

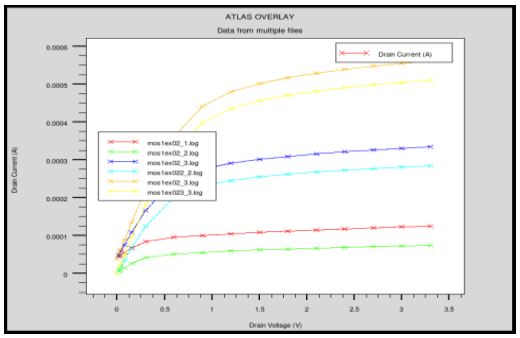

Figure 15: Result for dose 2E27

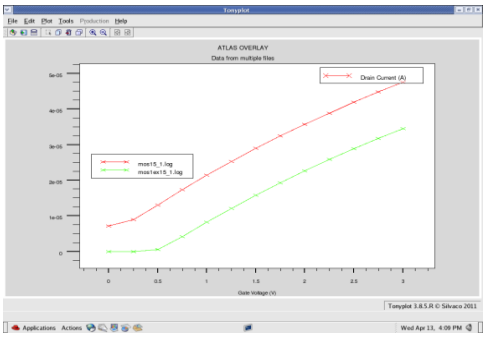

Figure 16: Result Ig /V_d for dose 1e25

4. Conclusion

In this paper, we have given an overview of radiation effects in Silicon-Germanium hetero junction bipolar transistors (SiGe HBT), BJT and GaAs/AlGaAs HBT & InP/InGaAS HBTs, HEMT, MOS and CMOS technology. We start by reviewing HBTs and study the impact of ionizing radiation with and without radiation. This effects are pronounced in SiGe HBT circuits ensure adequate tolerance for many orbital missions. SiGe HBT, GaAs HBT & InP HBT, HEMTs technology thus offers many interesting possibilities for electronic systems than widely used MOS and CMOS technology.

Acknowledgement

The author wishes to acknowledge Prof. A. Shastri for guiding and providing research facilities at Banasthali University. The author (CPJ) is grateful to Department of Science and Technology, New Delhi for supported this work through SERC grant.

References

[1] J. P. Colinge, "Hardening Integrated Circuits against Radiation Effects," IEEE NSREC 1997 *Short Course* Tutorial.

[2] P.Buchman, "Total dose hardness assurance for microcircuits for space environment," IEEE Trans. Nuc.Sci., vol.NS-33, p.1352, Dec 1986.

[3] A.H. Johnston, B.G. Rax and C.I. Lee, "Enhanced damage in linear bipolar integrated circuits at low dose rate," IEEE Transactions on Nuclear Science, vol. 42, no. 6, pp. 1650-1659, 1995.

[4] P.W. Marshall, M.A. Carts, A. Campbell, D. McMorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert, and R.A. Reed, "Single event effects in circuit-hardened SiGe HBT logic at gigabit per second data rates," IEEE Trans. Nucl. Sci., vol. 47, pp. 2669-2674, 2009.

[5] M.E. Kim et al., "GaAs Heterojunction Bipolar Transistor Device and IC Technology for High performance Analog and Microwave Application,"IEEE Trans. Microwave Theory Tech., vol.37, pp. 1286-1303, 1989.

[6] S. Blayac, M. Riet, J. L. Benchimol, F. Alexandre, P. Berdaguer, M. Kahn, A. Pinquier, E. Dutisseuil, J. Moulu, A. E. Kasbari, A. Konczykowska, and J. Godin, "MSI InP/InGaAs DHBT technology: Beyond 40 Gbit/s circuits," in Proc. 14th Indium Phosphide Related Materials Conf., vol. B1-4, Stockholm, Sweden, May 2002, pp. 51–54.

[7] Y. S. Puzyrev, T. Roy, Student Member, IEEE, E. X. Zhang, Member, IEEE, D. M. Fleetwood, Fellow, IEEE, R. D. Schrimpf, Fellow, IEEE, and S. T. Pantelides, Member, IEEE", Radiation-Induced Defect Evolution and Electrical Degradation of AlGaN/GaN High-Electron-Mobility Transistors", IEEE Transactions on Nuclear Science, Vol. 58, No. 6, December 2011.

[8] P. E. Dodd, Fellow, IEEE, M. R. Shaneyfelt, Fellow, IEEE, J. R. Schwank, Fellow, IEEE, and J. A. Felix, Member, IEEE", Current and Future Challenges in Radiation Effects on CMOS Electronics", IEEE Transactions on Nuclear Science, Vol. 57, No. 4, August 2010.

[9] Rajan Arora, Eddy Simoen, En Xia Zhang, Daniel M. Fleetwood, Ronald D. Schrimpf, Kenneth F. Galloway, Bo K. Choi, Jerome Mitard, Marc Meuris, Cor Claeys, Anuj Madan, and John D. Cressler", Effects of Halo Doping and Si Capping Layer Thickness on Total-Dose Effects in Ge p-MOSFETs", IEEE Transactions on Nuclear Science, Vol. 57, No. 4, August 2010.

C. P. Jain has received his B.E degree in EIC Engineering from Govt. Engineering College Kota (University of Rajasthan) in 2000 and M.Tech in VLSI Design from UP Technical University Lucknow and submitted PhD in Microelctronics. He has a more than 12 year teaching and research experience and 2 year Industrial Experience. Currently working as an Assistant Professor in EIC department at Govt. Engineering College Ajmer. He has presenting several papers in international & national conferences and guided 29 M.Tech dissertations. He has publish many research book and working on many government funded research projects. His research interests include design and development of semiconductor devices and circuits in Extreme environments, Analog and mixed signal design, physical design-ASIC design.