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Harmonic Analysis and Design of Embedded Z-Source Inverter for Induction Motor Drives

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Abstract

This Project deals with an Embedded Z-source inverter to control the three phase induction motor. The Z-source inverters are recent topological options for buck–boost energy conversion with a number of possible voltage and current-type circuitries. The common advantage of Z-source inverter and Embedded Z-source inverter is the inclusion of an LC impedance network, placed between the dc input source and inverter bridge. The drawbacks of the conventional Z-source inverters are more harmonic, less reliable, more diode blocking voltage and capacitor size also high. By introducing Embedded Z-source inverters, the drawbacks of the conventional Z-source inverter can be eliminated and also gain produced is same as that of Z-source inverter. It can produce smoother and smaller current or voltage maintained across the dc input source without using any additional passive filter, less cost and low harmonic distortion. The project is further carried to control the induction motor drive which is used in paper mills, textile mills and cement industries etc.

Keywords

Embedded Z-source inverters, motor drives, buck-boost, Z-source inverters.

1. Introduction

The Inverter is the circuit, used to convert the direct current input signal into alternating current output signal. Traditionally there are three types of inverters namely Voltage Source Inverter, Current Source Inverter and Z-source Inverter. In this thesis, the Z-Source Inverter is considered in place of Voltage Source Inverter and Current Source Inverter, because the drawback of conventional voltage source and current source inverter can be eliminated by using Z-source inverter. The main advantages of the Z-source inverter are to improve the voltage level of the inverter input voltage, reduce the voltage spikes and current spikes in the output. The efficiency of the inverter is highly improved through our project by means of the proposed Embedded Z-source inverter technique.

A Z-source inverter, first proposed in [1] as shown in Figure 1, as the single-stage inverter topology to demonstrate both buck and boost power conversion ability. Various Z-source topological options have been developed with either voltage-type or current-type conversion ability [1], [2]. Among them, the voltage-type inverters are more popular which are tested for applications in motor drives [3]–[6] and fuel cell- [6]–[9] and photovoltaic (PV)- [9]–[11] powered systems. The operational mode characteristics present in the Z-source inverter has been developed [14] using small inductance and low power factor. For controlling the Z-source inverters, many pulse width modulation schemes [12], [13] have also been reported with some achieving a lower switching loss and others realizing an optimized harmonic performance. The mathematical analysis of the Z-source inverter [15]-[17] is same as that of mathematical model of the Embedded Z-source inverter.

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2. Z-source inverter

The voltage-type Z-source inverter is shown in Figure 1. Where an X-shaped *LC* impedance network is connected between the input dc source with a diode and three-phase inverter bridge. With the impedance network added, any two switches from the same phase-leg can now be turned on safely to introduce a shoot-through or short-circuit state with no surge in the current observed, since all the paths taken by the current in the dc front-end are entirely limited by at least an inductive element (L_1, L_2, or both). In response to the inserted shoot-through state, the Z-source inverter can then be proven to exhibit voltage-boosting capability, whose corresponding gain expression is derived by considering the inverter-state equations during the occurrence of shoot-through and non the shoot-through states, expressed by (1)–(4) with the use of a balanced network assumed (L_1= L_2= L and C_1= C_2= C). Note that for the case of non-shoot-through state, it can represent any of the active states that are traditional and total of six ($i_i \neq 0$) or the remaining of the two null states ($i_i = 0$), solely determined by the modulation process.

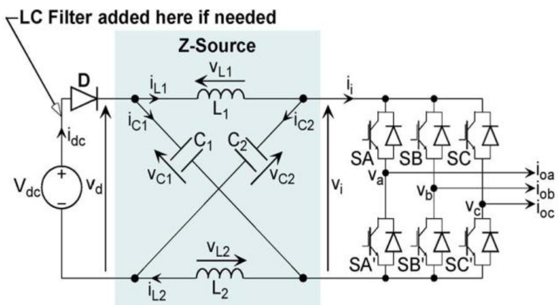

Figure 1: Z-source inverter

Shoot-Through($S_x = S_x^{'}$ ON, x = A, B, or C; D = OFF)
$V_L = V_C$ $V_i = 0$ $V_d = 2V_C$
$V_D = V_{dc} - 2V_C$ (1)
$I_L = -I_C$ $I_i = I_L - I_C I_{dc} = 0.$ (2)
Non-shoot-Through ($S_x \neq S_x^{'}$, x = A, B, or C; D = ON)
$V_L = V_{dc} - V_C V_i = 2V_C - V_{dc} V_d = V_{dc}$
$V_D = 0$ (3)
$I_{dc} = I_L + I_C$ $I_i = I_L - I_C I_{dc} \neq 0$ (4)
Performing state-space averaging on (1) and (3) then results obtained from the following expressions which are derived for the calculation of capacitive voltage V_C, peak dc-link voltage V_P, and peak ac output voltage V_{ac}.

$$V_c = \frac{1 - T_o/T}{1 - 2T_o/T} V_{dc} \quad (5)$$

$$V_p = \frac{V_{dc}}{1 - 2T_o/T} \quad (6)$$

$$V_{ac} = M \frac{V_P}{2} \quad (7)$$

where *T0/T* refers to the shoot-through ratio (T_0/T <0.5)for a single switching period, *M* denotes the modulation index that is used for traditional inverter control, and $B = 1/(1 - 2T_0/T)$ is the boost factor. Clearly, the term enclosed by the parentheses in the expression for V_{ac}represents the output amplitude produced by a traditional VSI, which can be boosted by raising *B* above unity and adjusting *M* accordingly.

3. Design of Z-source inverter

The conventional circuit consists of various modes of operation which include ordinary inverter mode operation and also in this circuit can be characterized mainly into two modes; there are shoot-through mode and non-shoot through mode. There is an inductive element placed along all current paths in the dc front-end, the switches from the same phase-leg can, as usual, be turned on simultaneously to introduce a shoot-through state without damaging semiconductor devices. In this mode capacitor can act as source of supply, the energy stored in the capacitor can be discharged though inductor, so it charges more. Figure 2 describes the equivalent circuit for the above mode. This circuit act as the two parallel LC circuit connected in series, the resultant frequency is expressed in the following manner.

$$f = \frac{1}{2\pi\sqrt{LC}} \text{ Hz} \quad (8)$$

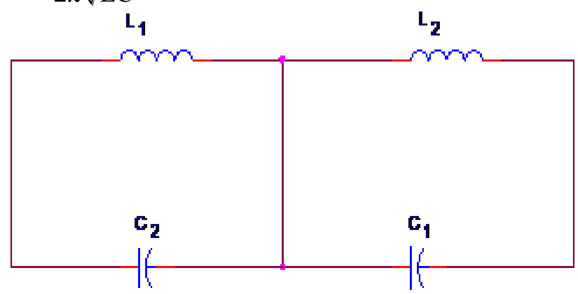

Figure 2: Equivalent circuit of shoot through mode

The shoot-through time period is 0.3ms.Using (8), choose any one parameter and find out another parameter. Using(8) C=1000µF, and L=2.3mH.

4. Embedded Z-source inverter

Comparing with Figure 1, the voltage-type EZ-source inverter shown in Figure 3 has its dc sources embedded within the X- shaped *LC* impedance network with its inductive elements L_1 and L_2 now, respectively, used for filtering the currents drawn from the two dc sources without using any external *LC* filter. The switches that are from the same phase-leg can be turned on simultaneously to introduce a shoot-through state without damaging semiconductor devices. The resulting equivalent circuit is shown in Figure 4(a), where it is shown that when the inverter bridge is in shot-through mode, the front-end diode D is reverse biased with its blocking-voltage expression and other state equations written as follows.

Shoot-Through($S_x = S_x^{'}$ ON, x = A, B, or C; D = OFF)
$V_L = V_C + V_{dc}/2$ $V_i = 0$

$V_d = V_D = -2V_C$ (9)
$I_L = -I_C \quad I_i = I_L - I_C$
$I_{dc} = 0.$ (10)

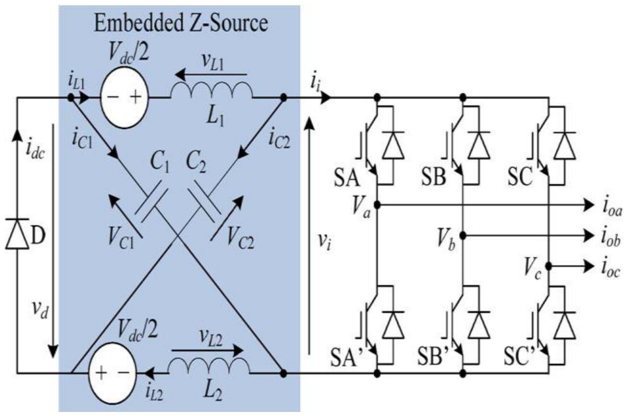

Figure 3: Embedded Z-source inverter

Non-shoot-Through ($S_x \neq S_x^{'}$, x = A, B, or C; D = ON)
$V_L = V_{dc}/2 - V_C \, V_i = 2V_C$
$V_d = V_D = 0$ (11)
$I_{dc} = I_L + I_C \quad I_i = I_L - I_C$
$I_{dc} \neq 0$ (12)

Performing state-space averaging on (9) and (11) then results obtained from the following expressions which are derived for the calculation of capacitive voltage V_C, peak dc-link voltage V_P, and peak ac output voltage V_{ac}.

$$V_c = \frac{V_{dc}/2}{1-2T_o/T} \quad (13)$$

$$V_p = \frac{V_{dc}}{1-2T_o/T} \quad (14)$$

$$V_{ac} = M\frac{V_P}{2} \quad (15)$$

where (18), when compared with (7), clearly shows that both Z- and Embedded Z-source inverters produce the same transfer gain even though the Embedded Z-source inverter has its dc sources embedded within the impedance network for achieving inherent filtering. Observing carefully, a second advantage is also noted in (16) when comparing its capacitive voltage $V_C$with that expressed in (5). To be specific, $V_C$in (13) is only a fraction of that in (5) with their ratio mathematically expressed as

$$\frac{V_{c(16)}}{V_{c(5)}} = \frac{1}{2(1-\frac{T_o}{T})} \quad (16)$$

Where the subscripts in (19) represent the numberings of the respective $V_C$expressions. Noting that T_0/T is always smaller than 0.5; the ratio in (19) is calculated to span from 0.5 to 1 as *T0/T* rises from 0 to 0.5, inferring that the second advantage introduced by embedding the sources is a significant reduction of the capacitor sizing (voltage rating). The reduction is as much as 50% under nominal condition during which *M* is set close to unity (or 1.15 if triplen offset is injected) and T_0/T is kept small.

5. Input-Source Requirement

Although the Embedded Z-source inverter shown in Figure 3 uses two independent dc sources to produce a balanced front-end impedance in the network but in practice, it is not required for both the sources to be balanced at all. In extreme cases, one or more sources can be omitted. The elimination of one source is a very favourable aspect to the industry, where locating a single source is definitely much easier. Relevant

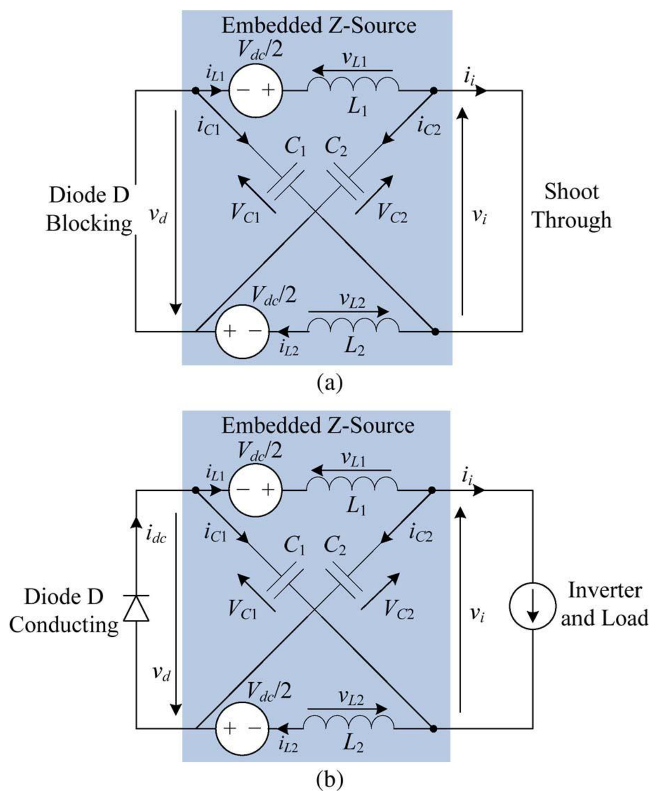

Figure 4: Equivalent circuit of Embedded Z-source inverter (a) shoot through state (b) non-shoot-through state

mathematical analysis and experimental testing for the case of only a single source powering the Embedded Z-source inverter have already been presented by the authors in [17], where the general concluded that when a single source is enough or sufficient, if the unbalanced voltage drops across the front-end passive *LC* elements are acceptable. In addition to [17], the same analysis can also be found in [18] and [19], which in principle are independent research papers reporting on the same topic and printed at about the same time in the same conferences.

6. Experimental Results

The embedded inverters proposed in this paper were verified experimentally using a hardware platform that could flexibly be configured to any desired topology for testing. Upon completing the tests, most of the captured results were observed to be the same, as proven conceptually in earlier sections.

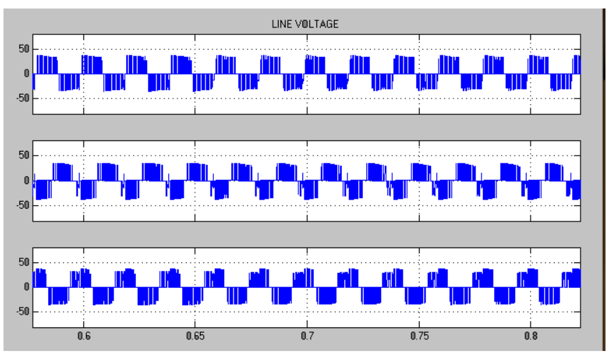

Figure 5(a): Experimental line voltage of Z-source inverter with T_0/T = 0.3

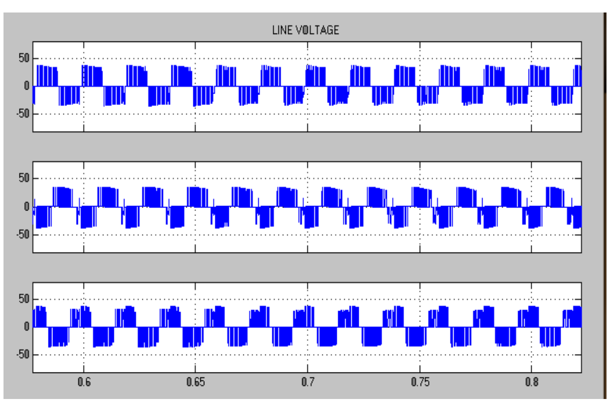

Figure 5(b): Experimental line voltage of Embedded Z-source inverter with T_0/T = 0.3

Therefore, to avoid excessive duplication, only results for the EZ-source inverters are presented here for illustration purposes. With an EZ-source network constructed using L =2.3 mH, C = 1000 μF, and $V_{dc} \approx$ 20 V and connected to a two-level voltage type inverter controlled by a micro controller, Figure 5 shows the relevant waveforms obtained by setting the relevant control parameters to M = 1.15 × 0.7 and a shoot-through duration of T_0/T = 0.3 added to the inverter-state sequence.

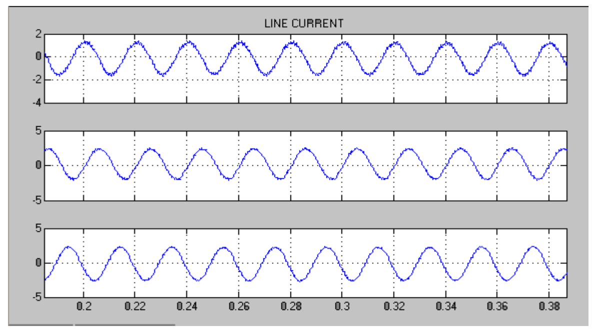

Figure 6(a): Experimental line current of Z-source inverter with M= 1.15 × 0.7 and T_0/T = 0.3

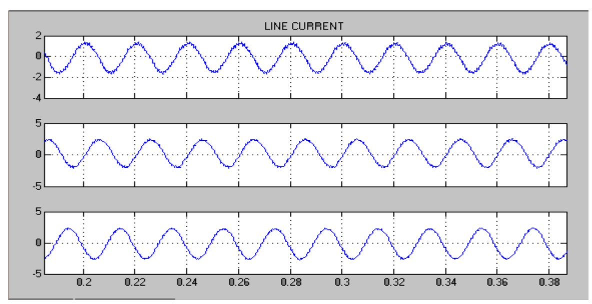

Figure 6(b): Experimental line voltage of Embedded Z-source inverter with M = 1.15 × 0.7 and T_0/T = 0.3

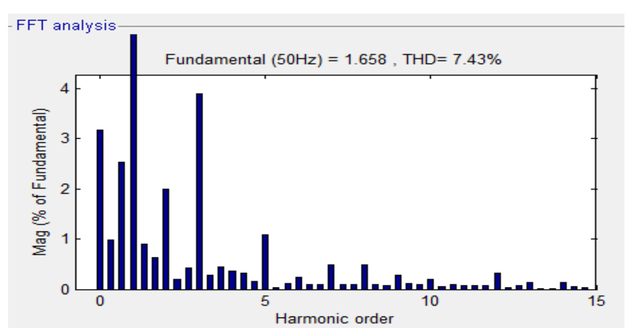

Figure 7(a): Total harmonic distortion of Z-source inverter

Figure 5(a), 5(b) clearly shows the boosting of line-voltage in both Z-source inverter and Embedded Z-source inverter. Figure 6(a), 6(b) clearly shows the boosting of output current in both Z-source inverter and Embedded Z-source inverter. Fig 7(a),7(b) shows that line current harmonic distortion of both Z-source inverter and Embedded Z-source inverter, which clearly implies the relation between percentage magnitude of fundamental harmonics and harmonic order. The Z-source and Embedded Z-source inverter can be used for current type inverter also.

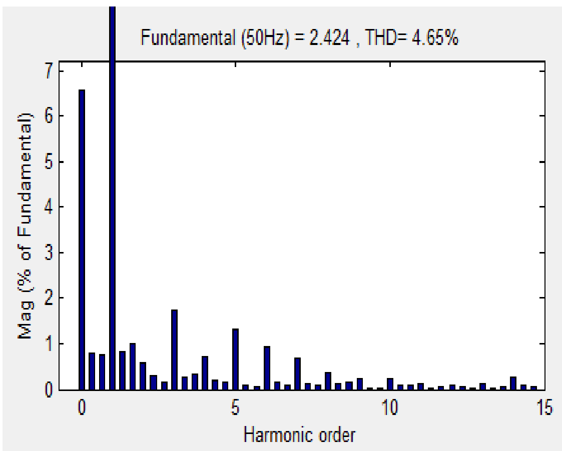

Figure 7(b): Total harmonic distortion of Embedded Z-source inverter

Table 1: Comparison Chart-Harmonic Analysis

Load	**1st harmonic**	**2nd harmonic**	**3rd harmonic**	**4th harmonic**	**5th harmonic**
0.0	100%	1.24%	0.77%	0.4%	0.31%
0.2	100%	1.2%	0.76%	0.46%	0.27%
0.4	100%	1.22%	0.76%	0.42%	0.29%
0.6	100%	1.25%	0.77%	0.39%	0.32%
0.8	100%	1.29%	0.78%	0.35%	0.35%
1.0	100%	1.32%	0.79%	0.32%	0.38%
1.2	100%	1.36%	0.80%	0.29%	0.40%

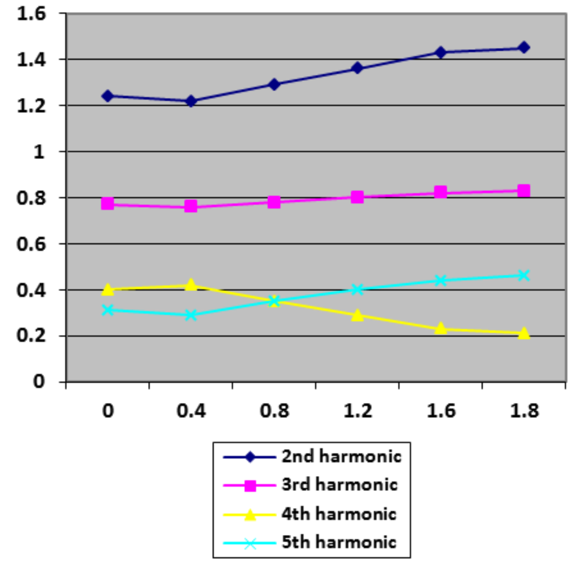

Figure 8: Graphical Representation -Variation of Harmonics at different load levels

7. Hardware setup

Figure8.clearly shows the hardware setup of the embedded Z-source inverter fed induction motor drives control. It consist of many sub modules namely power supply circuit, Impedance network, Driver circuit, and Inverter. This impedance network includes the direct current source, so this circuit named as Embedded Z Source inverter.

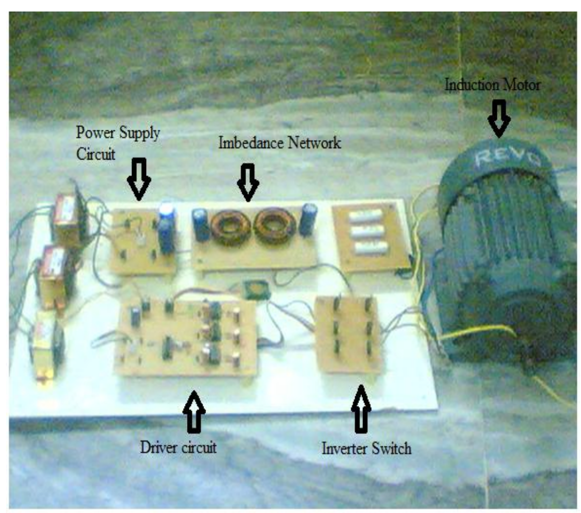

Figure 9: Hardware setup of Embedded Z-source inverter

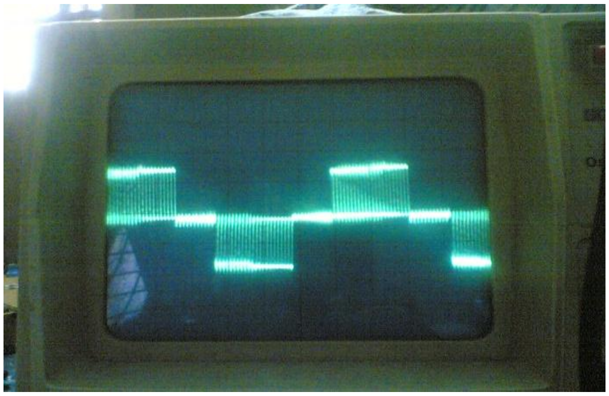

Figure 10: Experimental Line voltage waveform

Table 2: Comparative summary between z-source inverter and embedded z-source inverter

Parameter	Z-source Inverter	Embedded Z-Source Inverter
Line voltage	80 Volts	85 Volts
Line current	4 Amps	4 Amps
Total harmonic distortion	7.43%	4.65%
Diode blocking voltage	5 Volts	1.5 Volts
Capacitor voltage	30 Volts	15 Volts

The tabular summarization of comparative evaluation between Z-source inverter and the Embedded Z-source inverter is presented in Table I.

8. Conclusion

This paper has proposed a new family of Embedded Z-source inverters implemented using an impedance network with the relevant dc sources embedded within. Comparing with the Z-source inverters, the Embedded Z-source inverters have the advantages of drawing a smoother current from the dc input sources without using external second-order filters and a lower required capacitive voltage. The testing of the inverters has been performed experimentally with favourable results obtained, hence confirming the practicality of the new Embedded Z-source inverters. Needless to say, the embedded concepts can also be applied to the current type inverter also.

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