

Low Power State Retention Technique for CMOS VLSI Design

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Abstract

Mobile computing and mobile communication applications which are powered by battery, the battery life is a major concern. Leakage power dissipation is critical in VLSI circuits as the battery leaks even when devices are in idle state. To reduce leakage power as well as total power in CMOS logic gates and circuits a new circuit technique called LPSR Technique is proposed in this paper. Earlier well known techniques for leakage reduction and state retention are compared with this technique. This technique reduces maximum amount of static leakage power during deep sleep mode, maximum power reduction during dynamic mode and has a provision of preserving state in low power sleep mode. All the circuits are designed; simulated and low power performance evaluation is done using CMOS technology files in Tanner EDA tool.

Keywords

Power dissipation, leakage currents, static power, state retention.

1. Introduction

Mobile computing and mobile communication applications which are powered by battery, the battery life is a major concern in designing. Leakage power loss is critical in Integrated circuits as it leaks the battery even when devices are in idle state. The on-going technology scaling has resulted in the use of low power supply voltages for CMOS circuits which have an associated effect of lower threshold voltages to improve performance. Since the channel length for successive technology generations is reducing, threshold voltage and gate oxide thickness are also

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being scaled down to keep pace with the performance. Low threshold voltage results in exponential increase in leakage current because transistors cannot be switched off completely [1]. Power dissipates in the form of heat.

For a CMOS circuit, the total power dissipation includes dynamic and static components. The components of static power dissipation are sub threshold leakage, junction leakage, gate oxide leakage, gate induced drain leakage, punch through leakage [1], [2].

Techniques like LECTOR [3], GALEOR [4], Sleepy Keeper [5], Sleepy Pass Gate [6], Low Power State Retention Technique (LPSR) are used for leakage control. Each method has its own advantages and disadvantages. Some techniques use dual VT transistors; high VT transistors to reduce leakage and low VT transistors to improve speed of operation in critical sections of the circuit.

The proposed LPSR technique reduces leakage power and total power in combinational circuits and data path elements, which makes use of single V_T transistors in all parts of the circuit to achieve low leakage power during sleep mode of operation and lower total power dissipation in Active mode. So comparing all the leakage control techniques this is the best technique to reduce total power dissipation.

2. Previous Techniques

LECTOR Technique

The LECTOR method inserts two extra Leakage Control Transistors (a P-type and an N-type) within the gate, in which the gate terminal of each Leakage Control Transistor is controlled by the source of the other. The effective stacking of transistors which increase the off resistance in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated based on the observation from “a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path”. The circuit diagram of a 2- input nand gate and block diagram using LECTOR technique is shown below.

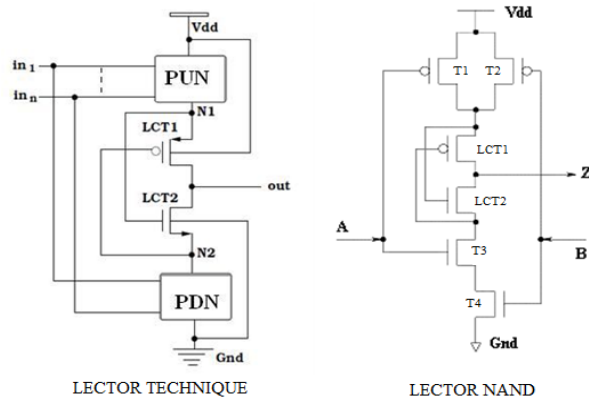


Figure: 1 LECTOR technique and its NAND implementation

GALEOR Technique

GALEOR technique reduces the leakage current flowing through the circuit for all possible input combinations by introducing stack effect. 2-input NAND gate using GALEOR technique is shown in the figure. In GALEOR technique, a leakage control high V_t NMOS transistor is placed between output and pull-up circuit and a leakage control, high V_t PMOS transistor is placed between output and pull-down circuitry.

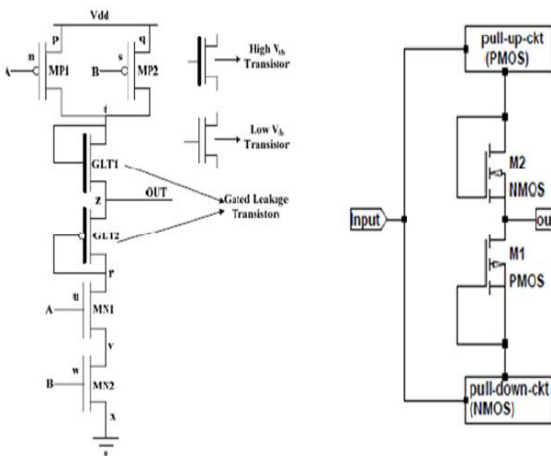


Figure: 2 GALEOR techniques and its NAND implementation

This technique reduces the output voltage swing due to the threshold voltage loss caused by the high V_t MOS transistors, and in turn increases propagation delay through the circuit. The main disadvantage in using these techniques is there is no sleep mode which increases static leakage power dissipation in

idle mode. In order to overcome these drawbacks sleepy keeper and sleepy pass transistor techniques are proposed.

SLEEPY KEEPER Approach

SLEEPY KEEPER uses a PMOS transistor in parallel to NMOS sleep transistor in the pull down path and NMOS transistor in parallel to PMOS sleep transistor in the pull up path. The extra retention transistors are connected to the output so that during sleep mode the logic state is maintained, but results in very high power dissipation.

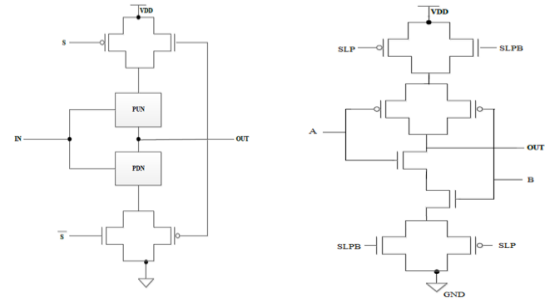


Figure: 3 Sleepy Keeper approach and its NAND implementation.

Sleepy Pass Gate Approach

In Sleepy-Pass Gate approach two sleep transistors PMOS and NMOS are connected in parallel and inserted between Pull-Up and Pull-Down Networks of a CMOS logic gate to form a pass gate like structure. This has large power dissipation during pulsed operation.

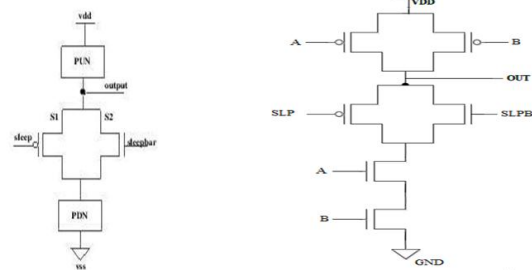


Figure: 4 Sleepy Pass gate approach and its NAND implementation

Even though the above discussed techniques reduce the power dissipation this techniques cannot retain state during sleep operation. So in this paper a novel low power state retention technique is proposed

where it retains the logical output state even in sleep mode.

3. Proposed Methodology

LPSR Technique

The LPSR technique uses a pair of NMOS and PMOS transistors above the pull up and below the pull down network of the CMOS circuit. General block diagram as well as schematics of LPSR NAND and NOR gates are as shown below. This technique has four modes of operation.

1. Active Mode: two sleep control signals namely $slp = 0$ and $slpb = 1$ are used to switch on the sleep transistors in leakage control block. Thus the virtual ground node VG is at ground potential and the virtual power node VP is at VDD.

2. Deep Sleep Mode: The sleep signals are held at $slp = 1$ and $slpb = 0$ states to switch off all the sleep transistors in both pull up and pull down leakage control blocks. Thus the actual power and ground path are disconnected virtually and the circuit experiences lower voltage across the nodes VP and VG.

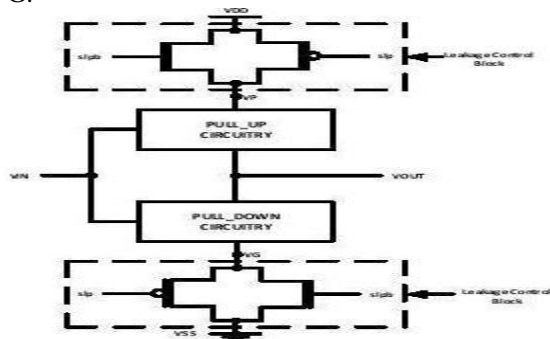


Figure: 5 LPSR approach

3. State Retention Mode 1: The sleep signals are given as $slp = 0$ and $slpb = 0$. The circuit sees a voltage higher than ground at the node VG and full VDD at the node VP. The state retention takes place with low leakage current with the output at good logic 1 level.

4. State Retention Mode 0: The $slp = 1$ and $slpb = 1$ are given as sleep control signals. The connection to actual ground is complete, the node VP is at lower VDD. Thus the state retention takes place with low leakage current with the output at good logic 0 level.

4. Simulation and Results

All the proposed techniques in this paper are designed for two input NAND gate and 2x1

multiplexer and simulated and functionally verified using 180nm CMOS technology files in Tanner EDA. Single VT transistors are used in all designs to show the performance benefits and comparison of different techniques. The logical functionality of gates is verified for all input combinations. Static power is calculated for all input combinations during active and sleep (idle) mode as well as dynamic power during clocked operations are all measured, and the delay analysis is done using EDA tools. The following figure shows the 2x1 Multiplexer circuit implemented using LPSR technique.

From the tables shown below we observe the dynamic power, static power for output logic-1 and logic-0 and the leakage power is less when compared LECTOR and GALEOR techniques. But slightly greater when compared to sleepy keeper approach and retains the state For LPSR technique the delay in active mode is less than all the approaches which increases the speed of the circuit. The following table shows the analysis for a 2x1 multiplexer.

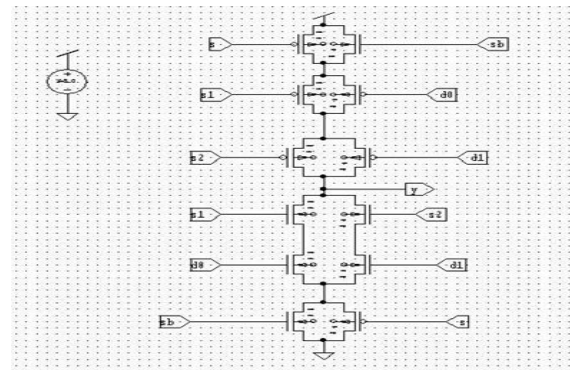


Figure: 6 Circuit Diagram of 2x1 multiplexer using LPSR technique

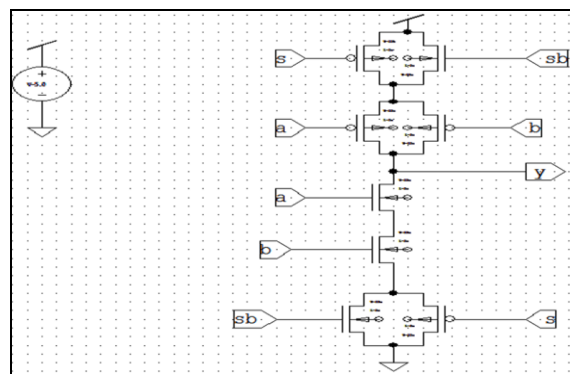


Figure: 7 Circuit Diagram of NAND gate using LPSR technique

Table 1: Delay and Power analysis of proposed techniques implemented using NAND gate

Technique	Dynamic power dissipation	Static power for logic 1	Static power for logic 0	Leakage power	Rise time	Fall time
Lector	849.43 μ w	5 77.01 pw	879.40 pw	NA	910.68ps	728.55ps
Galeor	1.01 nw	895.59 pw	56.01 pw	NA	910.68ps	1.27 ns
Sleepy keeper sleep mode	5.54 nw	5.59 nw	93.39 pw	134.42 pw	1.27 ns	910.68ps
Sleepy keeper active mode	217.36 pw	75.28 pw	286.77 pw	NA	1.27 ns	1.46 ns
Sleepy pass sleep mode	1.25 nw	-140.90 pw	886.96 pw	295.44 pw	910.68ps	910.68ps
Sleepy pass active mode	943.73 pw	1.01 nw	292.71 pw	NA	910.68ps	1.27 ns
Lpsr sleep mode	216.0 pw	75.28 pw	286.77 pw	NA	1.09 ns	1.27 ns
Lpsr deep active mode	2.56 nw	4.62 nw	93.39 pw	NA	10.68 ps	910.68ps
Lpsr state retention model	834.67 pw	547.40 pw	717.04 pw	NA	1.09 ns	1.09 ns
Lpsr state retention mode 0	4.72 nw	2.20 nw	289.24 pw	NA	1.27 ps	1.09 ns

Table 2: Delay and Power analysis of proposed techniques implemented using 2x1 multiplexer

Technique	Dynamic power dissipation	Static power for logic 1	Static power for logic 0	Leakage power	Rise time	Fall time
Lector	304.48 pw	404.43 pw	142.48 pw	1.45 mw	910.68 ps	1.09 ns
Galeor	293.29 pw	1.10 nw	-70.31 fw	722.74pw	1.46 ns	1.27 ns
Sleepy keeper active mode	10.29 pw	480.89 pw	68.71 pw	210.32pw	1.27 ns	1.27 ns
Sleepy keeper sleep mode	217.36 pw	75.28 pw	286.77 pw	NA	1.27 ns	1.46 ns
Sleepy pass active mode	1.25 nw	-140.90 pw	886.96 pw	295.44pw	910.68 ps	910.68 ps
Sleepy pass sleep mode	943.73 pw	1.01 nw	292.71 pw	NA	910.68 ps	1.27 ns
LPSR active mode	5.56 pw	141.52 pw	140.87 pw	NA	1.02 ns	1.02 ns
LPSR deep sleep mode	10.78 pw	478.63 pw	68.71 pw	NA	947.11 ps	947.11 ps
LPSR state retention model	438.37 pw	144.55 pw	155.67 pw	NA	1.09 ns	1.09 ns
LPSR state retention mode 0	583.83 μ w	2.13 nw	143.67 pw	NA	1.09 ns	947.11 s

5. Conclusion

LECTOR and GALEOR technique provide less dynamic power dissipation and more leakage power during active mode. But the main disadvantage is absence of sleep mode operation. The Sleepy Keeper approach maintains state during sleep mode at reduced level but results in large power dissipation during clocked operation because the output terminal is permanently connected to leakage control circuit and there is no deep sleep state. The Proposed LPSR technique has active mode static power on par with sleepy techniques and the least static power during deep sleep state and good state retention at low power. Thus the LPSR technique provides new methodology for the designers of low power VLSI circuits.

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