International Journal of Advanced Technology and Engineering Exploration
ISSN (Print): 2394-5443 ISSN (Online): 2394-7454
Volume-2 Issue-6 May-2015

Analysis of bridgeless single phase boost converter based on the three-state switching cell topology with feedback loop

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Abstract

The main aim of the project is to correct the power factor in single phase bridgeless converter. The AC-DC converters is used to improve power quality in terms of power factor correction, reduced total harmonic distortion at input AC mains and precisely regulated DC output. Here we introduce a bridgeless single phase boost converter based on three-state switching cell topology, whose distinct advantages are reduced conduction losses with the use of magnetic elements with minimized size, weight and volume. Boost converters operating in continuous-conduction mode is preferred because reduced electro-magnetic interference levels result from utilization. The principles of interleaved boost can also be employed. The feedback loop introduce from the load to the switching cell is to improve the power factor is also introduces in this paper. These converters are suitable for high power application due to present of auto transformer.

Keywords

AC-DC converters, Boost converter, power factor, three-state switching cell, type-3 compensator.

1. Introduction

A family of DC-DC converter topologies with three state switching cell converters was propose, one DC-DC boost topology was chosen to apply in power factor correction. Thus, the input DC source was replaced by input AC source followed by full-bridge diodes, The converter with an AC sources present the following advantages; capable to operate with high power, high efficiency in hard switching, reduced input and output current ripples; smaller input inductor and output capacitor; low weight and reduced volume.

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AC-DC converter of electric power is used in several applications such as adjustable-speed drives, switch-mode power supplies, uninterrupted power supplies (UPS), and battery energy storage. Conventionally, AC-DC converters mostly referred as rectifiers are implemented using diodes and thyristors to provide controlled and uncontrolled DC power with unidirectional and bidirectional power flow. The main drawbacks here include poor power quality in terms of injected current harmonics, resulting in voltage distortion and poor power factor(PF) at the input ac mains and slow varying rippled dc output at the load end, low efficiency and large size of AC and DC filters.

The reduction of harmonic content with the consequent of power factor can be obtained by using either passive or active power factor correction techniques. Passive methods include the use of tuned LC filters, represent a robust solution, However, increased size, weight, and volume. Moreover, the passive filter may not respond adequately if the load power factor comes to vary. Active methods come as a more efficient solution by using controlled solid-states switches in association with passive elements such as resistors, inductors and capacitors.

In order to meet the requirements in the proposed standards such as IEC 6100-3-2[1] and IEEE 519[2] standard on the quality of the input current that can be drawn by low-power equipment, a power factor correction circuits is typically added as a front-end stage. The boost power factor correction circuit operating in continuous-conduction mode (CCM) is used for medium and high-power applications. The continuous nature of the boost converter's input current result in low conducted electromagnetic interference (EMI) compared to other active power factor correction topologies.

Several issues must be taken into account to determine which types of static power converter is most recommended for a given application, such as robustness, power density, efficiency, cost and complexity[3]. Boost converter for PFC has

introduced in reverse-recovery problem for the boost diode[2],[3] and increasing of the output voltage[4].

As the power rating increases, it is often required to associate converters in series or in parallel. In high-power applications, interleaving of two boost converters is very often employed to improve the performance and reduce the size of the power factor correction front end. The current through the switch sometimes its becomes just fraction for high current application[5]. Interleaving effectively doubles the switching frequency and also partially cancels the inputs and output ripples, as the size or energy-storage inductors and differential-mode electromagnetic interference filters in interleaved implementation can be reduced[6].

A three-state switching cell (3SSC) can be obtained by the association of two two-state switching cells (2SSCs) interconnected to a center-tapped autotransformer, from which a family of dc-dc converters can be derived[7]. The first topology introducing 3SSC is in [8]. It is obtained by replacing the input source of DC-DC boost converter by a typical single-phase diode bridge and an AC voltage source. The presence of the diode bridge causes conduction losses to increase, because the current always flows through four semiconductor elements[1]. High output voltage gain by using 3SSC for DC-DC converter is achieved[9].

2. Basic operation

This paper introduces a topological variation of the boost converter based on the 3SSC for PFC applications. Four switches and two 3SSCs are used, making this converter suitable for high-current and high-power applications[1]. Moreover, the following advantages can be addressed to the use of the three-state cell: Inductors are designed for twice the switching frequency, with consequent reduction of size and weight; the current through the switches is half of the input current[9]; part of the input power is delivered to the load by the transformer instead of the main switches, consequently reducing conduction and commutation losses; lower cost switches can be used due to the possibility of parallelism of any number of cells; and the presence of the diode bridge is eliminated. The converter operation in both overlapping mode(OM) and non-overlapping mode(NOM) depend upon the value of duty cycle, if D>0 it is operate in overlapping mode and if D<0 it is operating in non-overlapping mode.[9]
The operation of continuous conduction mode (CCM) in non-overlapping mode are discuss as follows

1st stage $[t_{0,}t_1]$:

First the switch S_1 is turned on and the switch S_2 is turned off. The current which passed through the inductor is divided into two parts which is in the ratio of 1:1. The first one flows through L_2 and D_{b2} with the energy being delivered to the load. The second one flows through $L_1$and S_1. The current through inductor L_b increase linearly till t_1. The impedance across the windings L_1 and L_2 are same, and the voltage across them are equal to half of the output voltage V_0. The path of the current which is return to it sources is occurs through anti-parallel diode across the switch $S_3$and S_4. When switch S_1 is turn off then the first stage is finished.

2ndstage $[t_{1\,,}t_2]$:

When the switch S_1 is turned off and the switch S_2 is still remained off. The voltage across L_b is inverted, diodeD_{b1} is forward biased and diode D_{b2} remains conducting. The energy which which is store in inductor L_b in the former stage is then transferred to the load. The current flows through L_1,L_2 in the given polarity causes the magnetic flow in the core to be null. Then the current returns to the sources analogously to the previous stage. When switch S_2 is turn on this stage come to an end.

3rdstage $[t_2, t_3]$:

As the circuit is symmetry this stage is similar to the first one. Although switch S_2 is on and $S_1$is remained off. Diode D_{b1} is conducting and diode D_{b2} is reversed.

4thstage $[t_3, t_4]$:

This stage is similar as said in the second stage, as the same equivalent circuit and operating condition is valid.

The circuit diagram and the waveform of the bridgeless boost converter is as shown below:

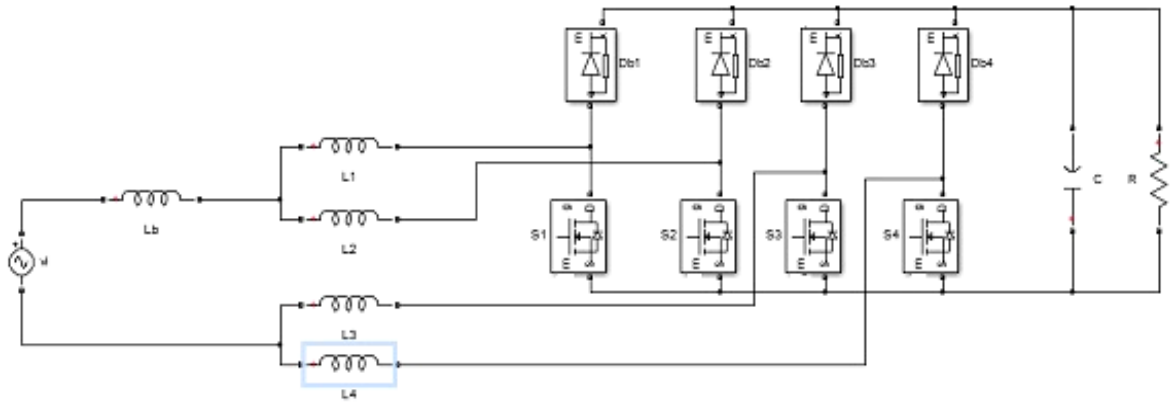

Fig 1: circuit diagram of bridgeless boost converter

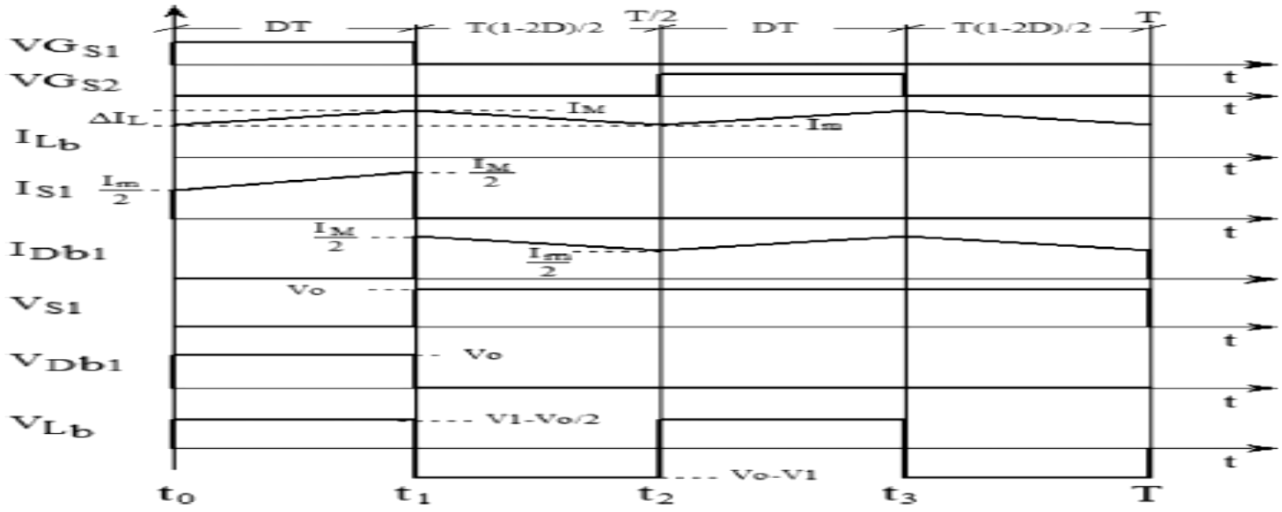

Fig 2: waveform of CCM-NOM

3. Type-III compensator

The error amplifier for frequency compensation can be a simple voltage-to-voltage amplification device that is the traditional Op-Amp. This type of Op-Amp requires local feedback to make it stable. The error amplifier can also be a voltage-to-current amplification device, that is, the gm Op-Amp. That is an open-loop amplifier stage with no local feedback. This application describes how to select the placement of compensation poles and zeros properly using Op-Amp and OTA for both Type-2 and Type-3 compensators.

The purpose of adding compensation to the error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could jeopardize the stability of the power supply. The ultimate goal is to make the overall closed-loop-transfer function (control-to-output cascaded with the error amplifier) satisfy the stability criteria. This is to avoid having the closed-loop phase any closer to 360 degrees than the desired phase margin anywhere the gain is greater than 1(0db). It is also desirable to have the slope of the gain curve at the crossover point with a value of -20db/decade. Phase margins of 45degrees to 60 degrees are considered safe values that yield well-damped transient load response.

Type-2 compensators are widely used in the control loops for power converters. When the phase lag of a power converter can approach 180 degrees, the maximal phase from a type-2 compensator at any frequencies is at most zero degree. Thus in these cases, the type-2 compensator cannot provide enough phase margin to keep the loop stable, and this is where a type-3 compensator is needed. A type-3 compensator can have a phase plot going above zero degree at some frequencies and therefore it can provide the required phase boost to maintain a reasonable phase margin.

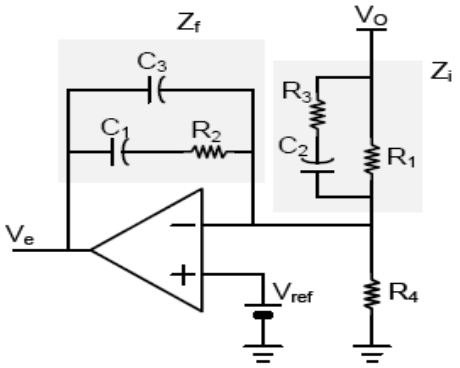

Fig 3: circuit diagram of Type-three compensator

the transfer function of the Type-3 compensator is given as

$$C(s) = \frac{V_0}{V_I} = \frac{(sC_2R_2+1)[sC_3(R_1+R_3)+1]}{R_1(C_1+C_2)s(sC_{12}R_2+1)(sC_3R_3+1)}$$

Where C_{12} is the series combination of C_1 and C_2,

$$C_{12} = \frac{C_1C_2}{C_1+C_2}$$

4. Design procedure of the converter

The specifications of the converter are shown in table-1

Table 1: Converter Specifications

Parameter	**Value**
RMS value of the rated input voltage	$V_i = 200V$
Grid frequency	f=60Hz
Input current ripple	$\Delta I_{lb} = 1.325$
Switching frequency	$f_s = 20KHz$
Rated output power	$P_0 = 1KW$
Output voltage	$V_0 = 400V$
Output Voltage Ripple	$\Delta V_0 = 10$
Expected theoretical efficiency	n=97%

A. Preliminary calculation.

Parameter α is the ratio between the output voltage and the peak input voltage[1]:

$$\alpha = \frac{V_0}{\sqrt{2}V_i} \dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

The angle that represents the transition between OM and NOM is:

$$\theta_1 = \sin^{-1}\left(\frac{\alpha}{2}\right) \dots\dots\dots\dots\dots\dots\dots (2)$$

The output current is

$$I_0 = \frac{P_0}{V_0} \dots\dots\dots\dots\dots (3)$$

A. Boost inductor

The boost inductance is given by:

$$L_b = \frac{T_s \cdot V_0}{16\Delta I_{lb}} \dots\dots\dots\dots (4)$$

The rms and peak currents through the boost inductor are given respectively by

$$I_{lb(rms)} = \frac{\sqrt{2}\ \cdot \alpha \cdot I_0}{\eta} \dots\dots\dots\dots\dots\dots (5)$$

$$I_{lb(peak)} = \frac{2 \cdot \alpha \cdot I_0}{\eta} \dots\dots\dots\dots\dots\dots\dots (6)$$

The core loss in the boost inductor can be obtained from

$$P_{lb(core)} = \Delta B^{2.4} \cdot (K_H \cdot f_{lb} + K_E \cdot f_{lb}^2) \cdot V_e = 0.036W \dots (7)$$

Where ΔB =0.04 the magnetic flux variation, $K_H = 4 \cdot 10^{-5}$ is the hysteresis loss coefficient.$f_{lb} = 2.f_s = 60KHz$ is the operating frequency of the boost inductor, $K_E = 4 \cdot 10^{-5}$ is the eddy-current loss coefficient, and $V_e = 42.5cm^3$ is the core volume.

The copper loss in the boost inductor is given by[9]

$$P_{lb(copper)} = \frac{\rho \cdot l_t \cdot N_{lb} \cdot I_{lb(rms)}^2}{n_{lb} \cdot S_f} = 0.976W$$

Where$\rho = 2.078 \cdot 10^{-6} ohm \cdot m$ is the copper resistivity at 70 degree centigrade, $i_t = 11.6cm$ is the average length of one turn, $N_{lb} = 30$ is the number of turns of the boost inductor,$n_{lb} = 5$ is the number of wire in parallel, and $S_f = 0.003255cm$ is the cross-sectional area of copper wire AWG22

The value for using is as shown table-2

Table 2: Power stage elements

Parameter	Value
Boost inductor	$L_b = 630\mu H$
Auto-transformer	$n_1 = 24, n_2 = 24$
Main switches	MOSFET 5015VBR
Boost diode	MUR460
Output capacitor	$C_0 = 780\mu F$
Load resistance	$R_0 = 160\Omega$

5. Software required

MATLAB/SIMULINK

MATLAB is a high level language and interactive environment for numerical computation, visualization, and programming. Using MATLAB we can analyses data, develop algorithms, and create models and applications. The language tools, and built-in math function enable us to explore multiple approaches and reach a solution faster than with spread sheets or traditional or traditional programming language .such as C/C++ or JAVA.

SIMULINK is a block diagram environment for multi-domain simulation and Model-Based Design. It supports system-level design, simulation, automatic code generation, and continuous test and verification of embedded systems. Simulink provides a graphical editor, customizable block libraries, and solvers for modeling and simulating dynamic systems. It is integrated with MATLAB enabling us to incorporated MATLAB algorithms into models and export simulation results to MATLAB for further analysis.

6. Simulation and results

The simulation and result of the bridgeless boost converter with and without the feedback loop have shown below:-

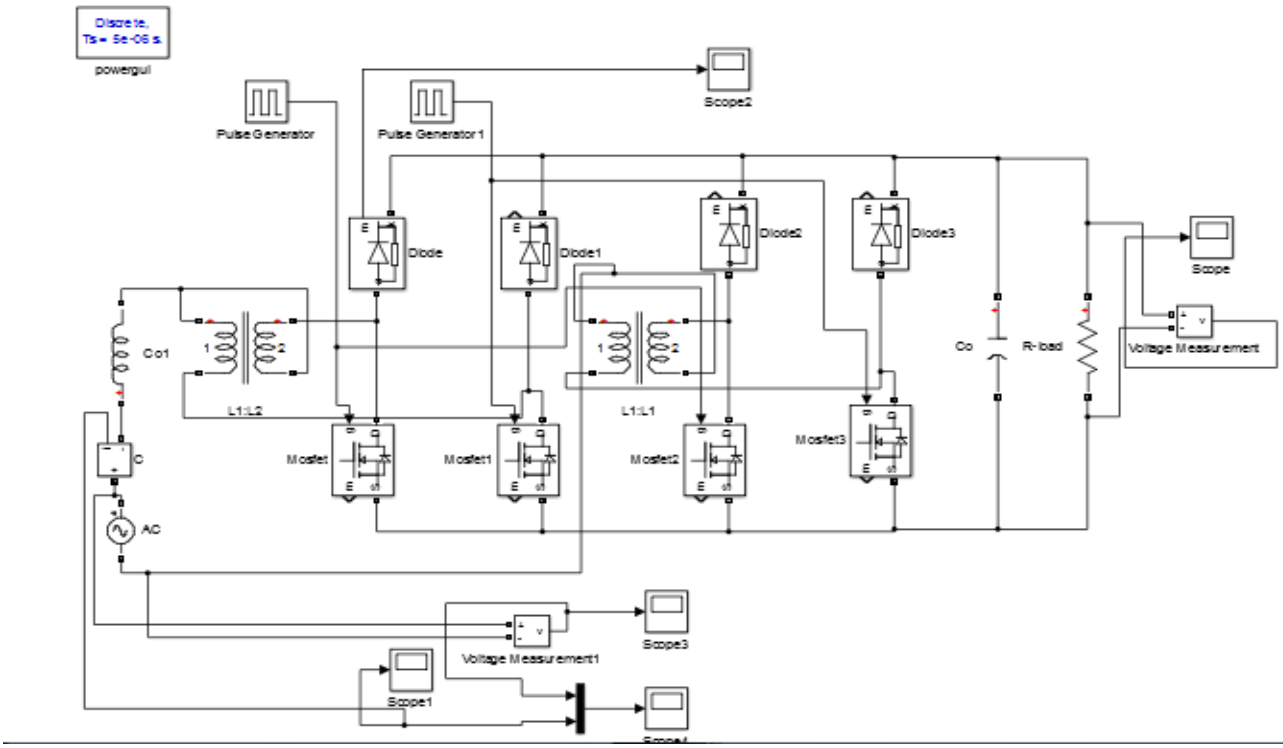

Fig 4: simulation diagram of boost rectifier employing the 3SSC

Fig 5: output waveform across R-Load

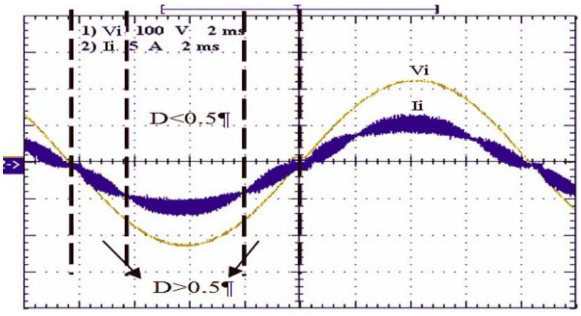

Fig 6: input voltage and input current $V_i =$ $100V$ and $P_0 = 650W$

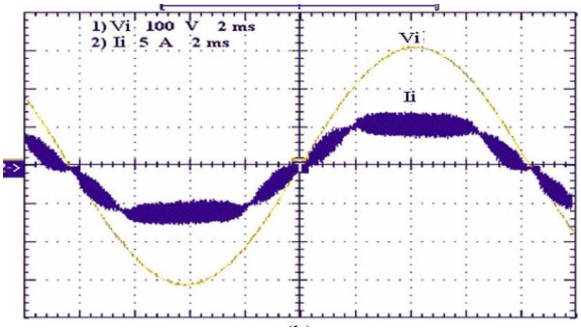

Fig 7: input voltage and input current $V_i =$ $220V$ and $P_0 = 1KW$

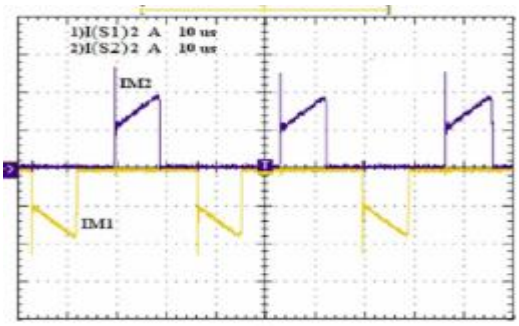

Fig 8: currents through switches S1 and S2 in non-overlapping mode

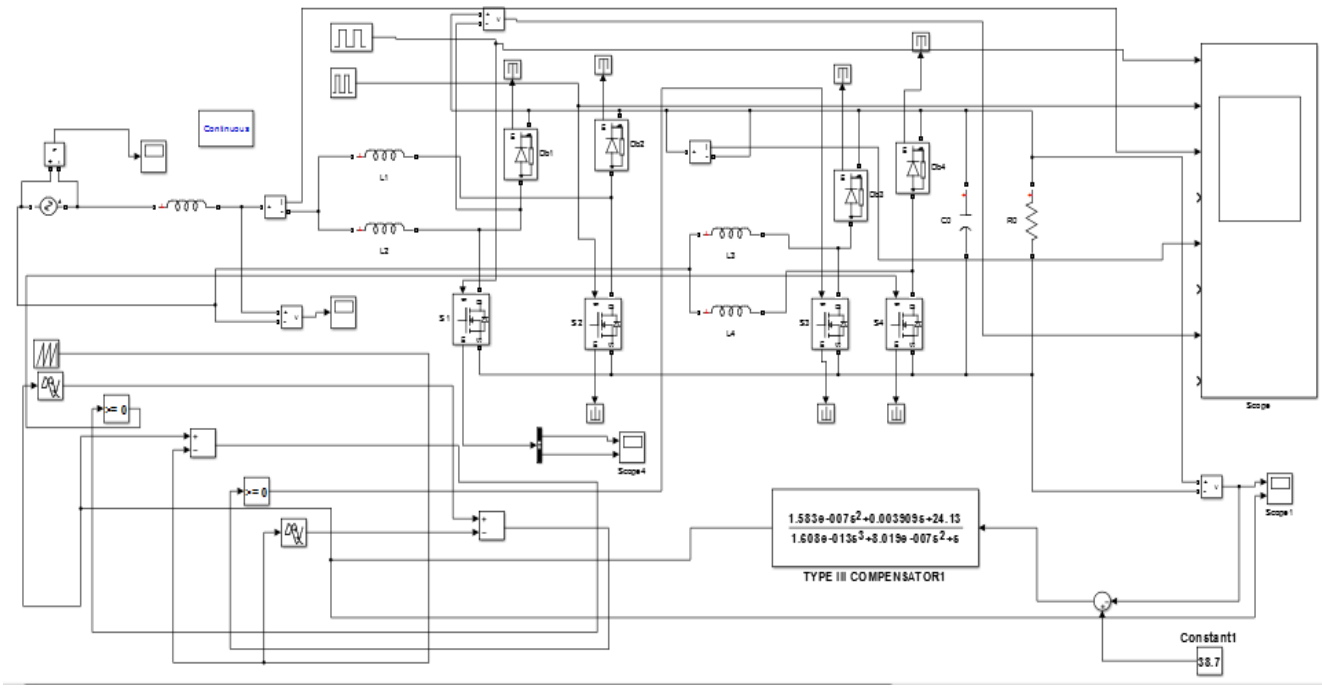

Fig 9: Simulation Diagram of boost rectifier employing the 3SSC

Fig 10: output waveform across the R-load and duty cycle of type-3 compensator

From the above fig we have seen the output voltage is increase in the bridgeless boost converter with the feedback loop. Increase in voltage then decrease in the current consumption to the load which conclude the power factor have improve compare to the bridgeless boost converter without feedback loop.

7. Conclusion

In this paper, the proposed of bridgeless boost converter three-state switching cell and type-3 compensator as the feedback loop reduced the conduction losses because the current flow through two power semiconductor in series of the converter. And only part of the energy from the input source flows through the active switches, while remaining part is directly transferred to the load without being process by these switches, that is, this energy is delivered to the load through passive components, such as the diodes and the transformer windings. For control loop different control techniques can also be used such as self-control[10], on cycle-control.

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