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Research Article

Area efficient SR flip-flop designed using 90nm CMOS technology

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Abstract
In this paper SR flip-flop is designed to reduce area and power using 90nm technology for efficient utilization of the circuit. This is done using digital schematic (DSCH) and microwind application. Two designs have been proposed for SR flip-flop, namely fully automatic and semicustom design. In fully automatic design inbuilt active devices are used along with auto routing and placements. In semi-custom design inbuilt active devices are used with optimized manual routing and placement. The proposed schematic in case of fully automatic approach is designed by using DSCH and its equivalent layout is created using microwind. While in the case of semi-custom approach optimized layout is created with microwind. It can be observed from the simulated results that power is reduced by 81% and area consumption is improved by 15% in case of semi-custom design as compared to fully automatic design.

Keywords
Area, CMOS FET, Layout, Power, Sequential circuits, SR flip-flop.

1.Introduction
The primary objective of this S-R flip-flop design is to reduce the area so that the circuit fits into the required integrated circuit chip efficiently. Secondarily, this paper also aims to reduce the power consumed by the circuit for efficient utilization of power provided to the integrated circuit chip. Sequential circuits are circuits in which output is determined by current inputs as well as past inputs and thus they require memory. The combinational circuit does not use any memory. Hence the previous state of input does not have any effect on the present state of the circuit. Sequential circuits have memory so output can vary based on given input. These type of circuits use previous input, output, clock and a memory element. Sequential circuit designs use flip-flops or latches, which are sometimes called memory elements that hold data. Sequential circuits are sorted as bistable, mono stable and astable. Bistable states have two stable states, either of them can be attained as per given conditions. Among the group of sequential circuits, the bistable circuits are the most popular ones. Timing elements such as latches, flip-flops, registers, and memory storage cells form the group of most important components in synchronous VLSI designs [1−2].

Very-large-scale integration (VLSI) is the procedure of making an integrated circuit (IC) by integrating many transistors into a single chip. All basic elements like flip-flops, registers and memory elements fall in this category [3]. Before the introduction of VLSI technology, ICs could perform limited set of functions. ICs have advantage of speed, size and power consumption over digital circuits. We have number of different IC fabrication technologies. The most important difference between technologies is the types of transistors they can produce [4]. MOSFETs offer the advantage of drawing almost zero control current while idle [5]. They come in two variants: pMOS and nMOS using n-type and p-type dopants respectively. An individual complementary metal–oxide–semiconductor (CMOS) transistor consumes very little energy each time it switches on; the huge amount of transistors switching at very high speed rate makes power utilization a major design consideration [6−10]. In this paper the estimation of SR flip-flop's performance is done based on area measured.

Section 2 discusses the SR flip-flop. Section 3 shows design schematic simulations; layout analysis is done in section 4 followed by result comparison in section 5 and concluded in section 6.

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2.SR flip-flop

The SR latch or SR flip-flop can be considered as a basic sequential logic circuit. This simple flip-flop is a one-bit memory bistable device that has two inputs, one which will "SET" the device (meaning the output = "1"), and is labelled S and one which will "RESET" the device (meaning the output = "0"), labelled R. The SR stands for "Set-Reset". The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level "1" or logic "0" depending upon this set/reset condition [11,12].

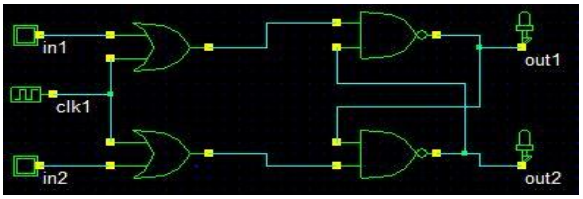

Figure 1 Clocked NAND based SR latch circuit

A basic NAND gate SR flip-flop circuit gives feedback through both its outputs back to its opposing inputs and is commonly used in memory circuits to store a single data bit [8]. Then the SR flip-flop actually has three inputs, Set, Reset and its current output Q related to its current state [6-7]. The word "Flip-flop" is related to the actual operation of the device, as it can be "flipped" into one logic Set state or "flopped" back to the opposing logic Reset state. The NAND based SR latch is implemented by combining the clock input as shown in *Figure 1*. The inputs (S and R) and clock signal (Clk1) are active low. It would mean that input signal will be nullified if clock is equal to logic '1' and those inputs will affect the outputs only when clock is active [13].

3.Schematic design simulation

After designing the initial schematic circuit in *Figure 1*, we test the running of this circuit in DSCH for further analysis. This testing is depicted in *Figure 2*.

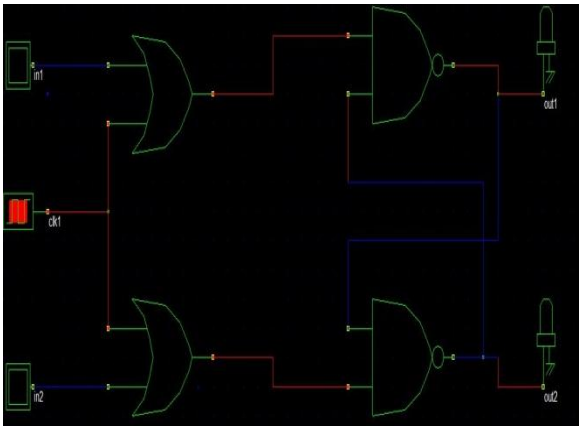

Figure 2 Simulation of NAND based sr latch circuit

Further, then we study the timing diagram of the circuit in DSCH and compare it with ideal circuit timing diagram. This generated timing diagram is shown in *Figure 3*.

Table 1 shows the theoretical truth table of SR flip-flop. In microwind, we simulate the file generated from the DSCH and get the voltage vs current graph for the circuit. This graph is shown in *Figure 4*.

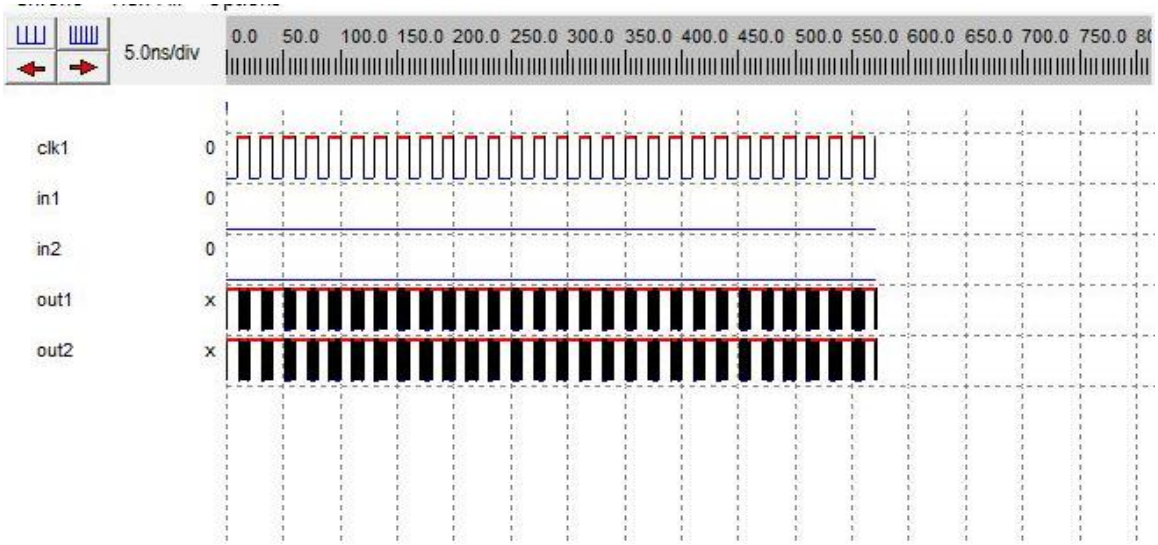

Figure 3 Timing diagram of fully automatic

Table 1 S-R flip-flop truth table

CLK	S	R	Q_N	$\bar{Q}_{N+1}$	Operation
0	0	0	0	0	Not allowed
0	0	1	1	0	Set
0	1	0	0	1	Reset
1	x	x	Q_n	$\bar{Q}_n$	Hold

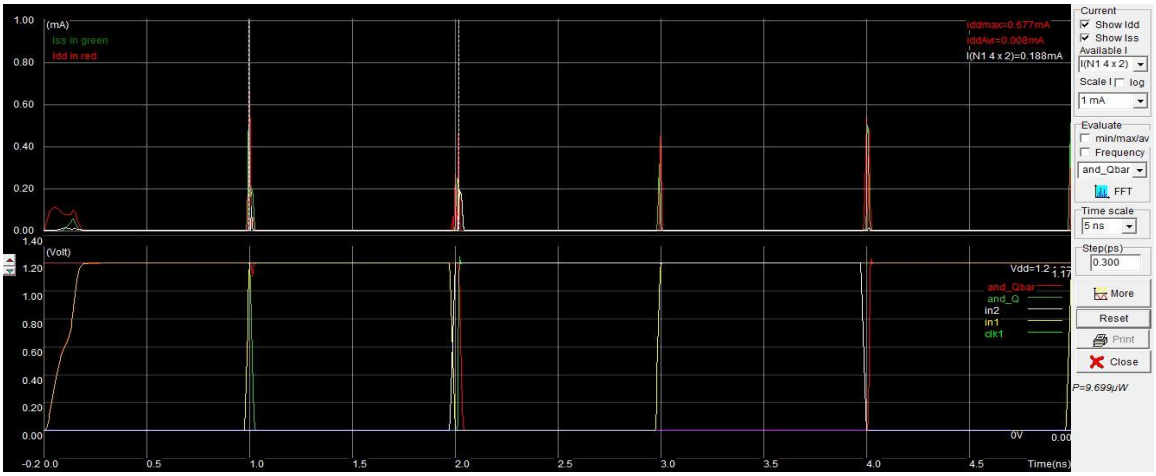

Figure 4 Voltage vs current graph

4.Layout design analysis

In the first method the schematic of SR flip-flop is designed, with the help of Microwind software the auto generated layout of SR flip-flop is created, afterwards simulation is done. In this, 90nm foundry is selected. The *Figure 5* represents the auto generated layout.

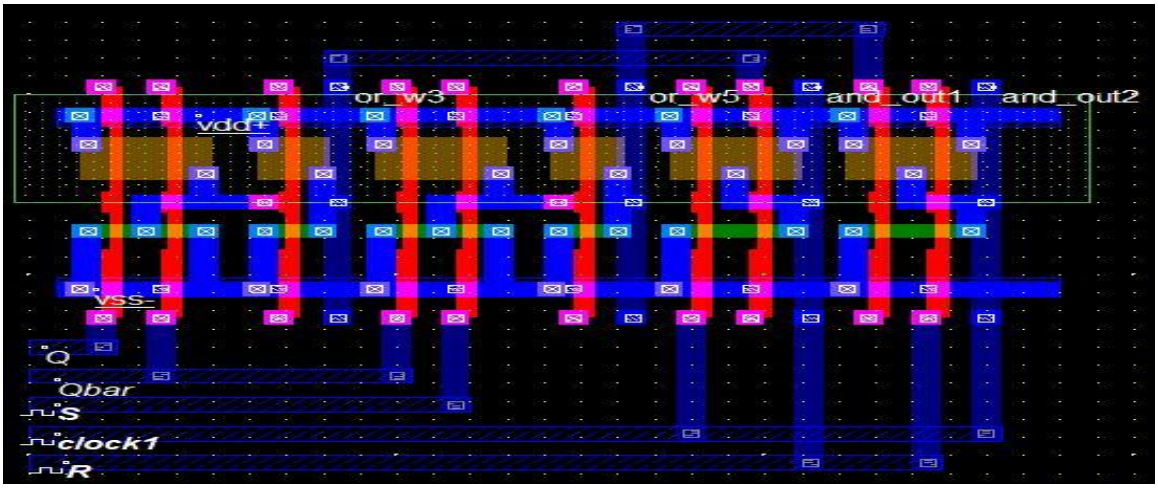

Figure 5 Fully automatic SR flip-flop

The layout is checked for DRC and if there no error is generated then simulated result appears. Later generated timing waveforms are verified by comparing to the circuit operation. The power generated is shown by the simulated result. The *Figure 6* shows the timing diagram of this automatic layout. The power and area consumed by this layout is measured. Here the consuming power is 9.699 µWatt. Area required for this particular layout is 65.2µm2 .Width is 8.8 µm and height is 7.4 µm. Secondly we prepare layout using semicustom approach. In semicustom approach the transistors are inbuilt, in this approach connections are made by following the lambda design rules. There is slight

possibility of power reduction. *Figure 7* represents the layout using semicustom approach. The semicustom layout is checked for DRC if there is no error present in layout, the circuit is simulated and timing waveforms are generated. The generated timing waveforms are verified with the truth table or operation of original circuit.

Figure 8 shows the timing diagram of semicustom layout. The power observed from this particular simulation, is 1.852 µWatt, more than automatic layout and area is calculated from the properties. Here the width is 6.8 µm (114 lambda) and height is 8.1 µm (135 lambda). In semicustom layout area is 55.4 μm^2. Voltage versus current graph is shown in *Figure 9*.

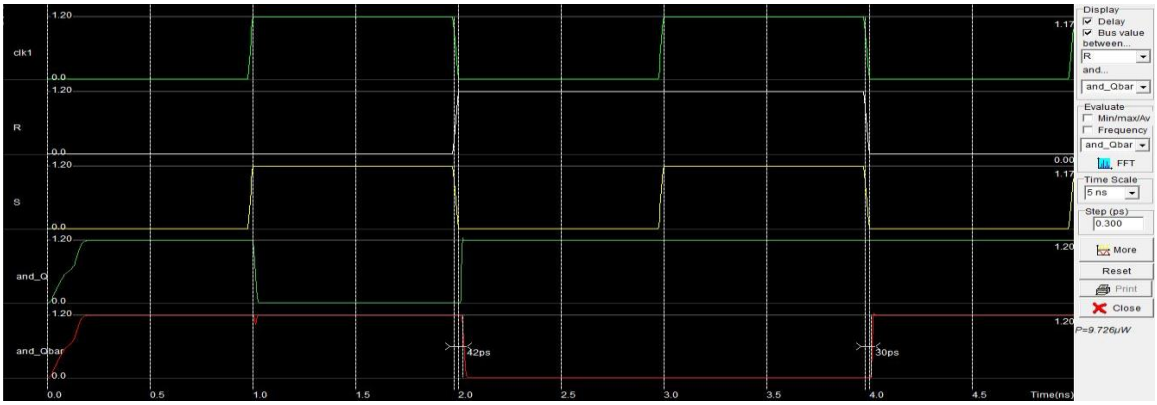

Figure 6 Timing diagram of fully automatic

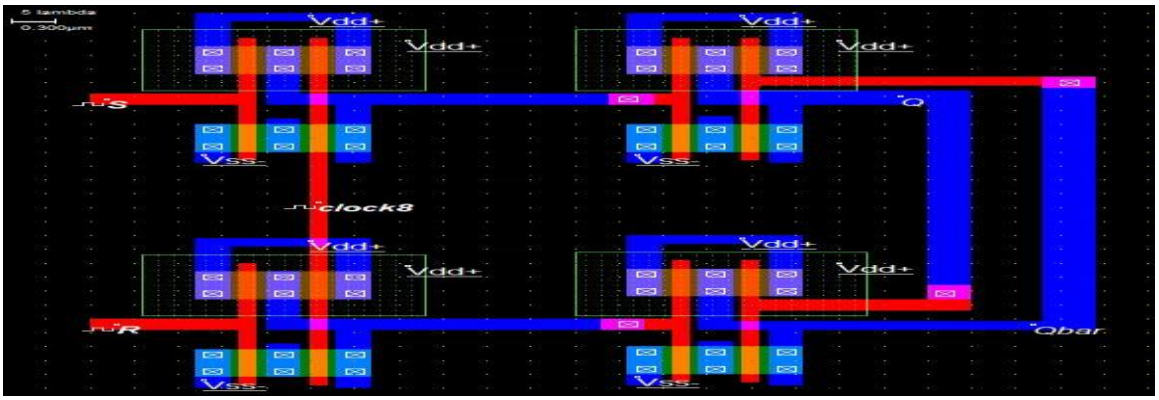

Figure 7 Semi custom SR flip-flop

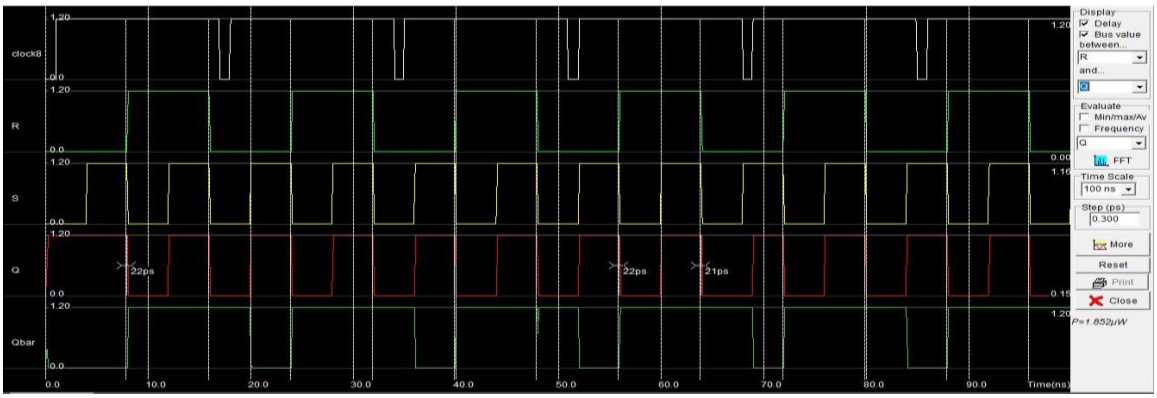

Figure 8 Timing diagram of semi-custom layout

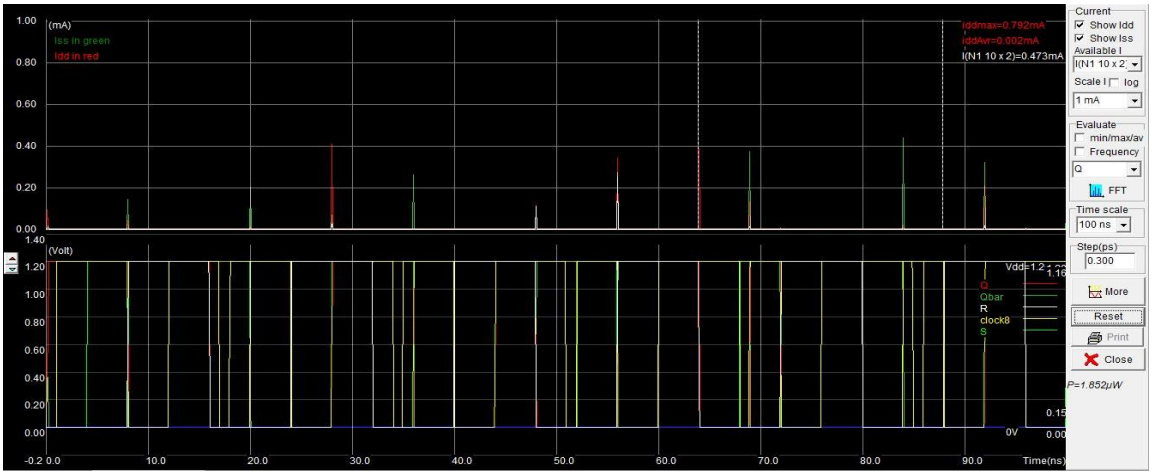

Figure 9 Voltage vs current graph

5.Result comparison

The performance of proposed semi-custom layout is compared with automated layout. The performance parameters being area and power.

Through above results a comparative study can be done between the two designing approaches.

Comparative analysis table (*Table 2*) shows that in terms of power the performance of semi-custom layout approach decreases. In terms of area and power both the semi-custom layout has better performance among the two design approaches.

Table 2 Comparison table

S. No.	Approach	Area(µM^2)	Power(µWATT)
1.	Fully Automatic	65.2 µm^2	9.699 µWatt
2.	Semi-custom	55.4 µm^2	1.852 µWatt

From the above comparison we observed, there is a reduction of 81% in power for semicustom layout generated in comparison to fully automatic layout and reduction of 15% in terms of area consumed. More area is required in auto generated approach. Comparative analysis in terms of area is done, which indicates that semi customized layouts have less area than auto generated [14, 15].

6.Conclusion

From the above result analysis it is clear that semi customized layout is better than auto generated layout by 7.847 µW in terms of power and 9.8 µm2 better in terms of area consumption. So this design approach can be implemented where power reduction is the main consideration. The future scope is to try designing the circuit as fully custom design in microwind and hence work on reducing its power consumption and area to make it work efficiently in the integrated chip. To compare the efficiency of fully custom design with these two design approaches and work on getting better results through fully custom design approach.

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Conflicts of interest

The authors have no conflicts of interest to declare.

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