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Performance Analysis of Silicon and Germanium Nanowire Transistor using Crystal Orientation and Oxide Thickness

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Abstract

Nanowire Transistors have attracted attention due to the probable high performance and excellent controllability of device current. In this paper, we investigate the performance analysis of nanowire transistors made of silicon and germanium materials. The nanowire transistor has a 3D distribution of electron density and electrostatic potential, therefore self-consistent 3D simulations are used. Nanowire (tool) is 3D Poisson self-consistent simulator which can study the 3D transport in nanowire transistor considering phonon scattering based on the effective-mass approximation. The output characteristics of the nanowire transistors are studied in detail for both Si and Ge materials for different transport orientation (i.e., 100,110,111) and varying the oxide thickness.

Keywords

Coupled mode space approach ;Uncoupled mode space approach;

1. Introduction

As traditional planar Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) are approaching nanometer scale, their performance becomes limited by Short channel effects (SCEs), increasing OFF-state current and poor electrostatic control of the channel [1]. Nanowires are nanoscale structures which are frequently single crystal materials and are typically cylindrical in shape. They can be formed in a variety of materials, including metallic (e.g., Ni, Pt, Au), semiconducting (e.g., Si, InP, GaN, etc.), and insulating (e.g., SiO2, TiO2), but are most frequently fabricated using semiconducting materials. Since semiconductors are used in transistors, semiconducting nanowires of silicon and germanium material are of the most interest. They have attracted attention not only because of their extremely small size, but because their size causes new physics (quantum effects) to apply, which do not occur classically, that can cause changes in material properties [2]. Three phenomena that are the most notable: (1) as the nanowire's diameter decreases, the energy band gap can change, (2) the nanowire's diameter can change the material's character [3], and (3) ballistic transport, i.e. without scattering, can occur which can lead to markedly improved device performance.

The reason which leads the researchers think about using nanowire transistor to replace of planar MOSFET is nanowire transistor has the strongest gate control over planar MOSFET and other proposed structures. However, at this time the nanowire transistor still is in its early stage, there is a lot of room to optimize the structure parameters and lots of new phenomenon to be explore by both experimental and computational approach, for instant, we need to determine the optimal diameter, the best material and the effect of random dopant or surface roughness or phonon scattering on its performance. In this work we have studied the output characteristics by different transport orientation (i.e., 100,110,111) and varying the oxide thickness in details for the nanowire transistor formed of silicon and germanium.

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2. Proposed Method

2.1. NEGF Formalism

The Simulation of electronic devices generally involves self-consistent solution of the electrostatic potential and carrier distribution inside the device. Over the years device engineers have improved our collective knowledge of carrier transport and semiconductor physics. Earlier treatment of electrons and holes as semi classical particles with an effective mass was good enough to predict semiconductor device behavior and the drift-diffusion equation was adequate to describe carrier transport.

Today, as we stand at 45 nm node and begin to enter 22 nm technology nodes, MOSFETs have shrunk to

nano scale dimensions, which have required a re-examination of our approach to device modeling. A more sophisticated analysis of the device physics is needed, such as the Non Equilibrium Green's Function (NEGF) approach, to model devices all the way to ballistic level (< 10 nm) [1][6]. The NEGF transport model is by far the most rigorous approach among existing quantum transport models and is the approach utilized in this modeling study.

2.2. Simulation Software Overview

The simulation software used for the modeling of nanowire transistors is based on the work done by Hong-Hyun Park *et al.* and his colleagues at Purdue University [4][5]. Nanowire (tool) is 3D Poisson self-consistent simulator which can study 3D nanowire transport considering phonon scattering based on the effective mass approximation. The calculation involves a self-consistent solution of a 3D Poisson equation and a 3D Schrödinger equation with open boundary conditions at the source and drain contacts. Using the finite element method (FEM), the 3D Poisson equation is solved initially to obtain the electrostatic potential throughout the device. At the same time, the 3D Schrödinger equation is solved by a uncoupled mode space approach, which provides both computational efficiency and high accuracy as compared with direct real space calculations.

3. Theory

To deeply understand device physics of nanowire transistors (NWTs) and to assess their ultimate performance limits, simulation work is necessary and important. In contrast to a planar MOSFET, which has a uniform charge and potential profile in the transverse direction (normal to both the gate and the source-to-drain direction),an NWT has a three-dimensional (3D) distribution of electron density and electrostatic potential. As a result, a 3D simulator is required for the simulation of NWTs. Figure 1 shows a schematic structure of the Si nanowire transistors simulated in this work.

In this paper, we propose a 3D self-consistent quantum simulation of NWTs based on the effective-mass approximation (whose validity in then an scale device simulation has been established in Ref. [7]). The calculation involves a self-consistent solution of a 3D Poisson equation and a 3D Schrödinger equation with open boundary conditions. Using the finite element method (FEM), we solve the 3D Poisson equation to obtain the electrostatic potential. At the same time, we solve the 3D Schrödinger by a (coupled/uncoupled) mode space approach which provides both computational efficiency and high accuracy as compared with direct real space calculations. Since the (coupled/uncoupled) mode space approach treats quantum confinement and transport separately, the procedure of the calculation is as follows:

- Solve the 3D Poisson equation for the electrostatic potential.
- Solve the 2D Schrodinger equation with closed boundary conditions for each cross section of the nanowire transistor to obtain the electron sub bands (along the nanowire) and eigen functions.
- Solve the coupled/uncoupled Non Equilibrium Green function (NEGF) transport equations for the electron charge density.
- Calculate phonon-electron interaction with the self-consistent born approximation.
- Go to step (1) to calculate the electrostatic potential. If the self-consistent loop has converged, calculate the electron current using the NEGF approach.

Different transport models (in Step 3) are implemented into our simulator. In this paper, we will discuss both ballistic NEGF model, which gives the upper performance limit of Si and Ge NWTs,and a dissipative NEGF model with a simple treatment of scattering with the Buttiker probes, which offer an efficient way to capture scattering in the quantum mechanical frame work.

3.1. Coupled Mode Space Approach

In this part of the work, we will briefly review the Coupled Mode Space (CMS) approach and list basic equations for our particular case of interest.In the 3D domain, the full stationery Schrödinger equation is given by

$$H_{3D}\Psi(x,y,z) = E\Psi(x,y,z) \quad (1)$$

Where, H_{3D} is the 3D device Hamiltonian. Assuming an ellipsoidal parabolic energy band with a diagonal effective-mass tensor (for the case that the effective-mass tensor includes non-zero off diagonal elements, please refer to Ref. [12]), H_{3D} is defined as

$$H_{3D} = \frac{h^2}{2m_x^*(y,z)}\frac{\partial^2}{\partial x^2} - \frac{h^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y^*(y,z)}\frac{\partial}{\partial y}\right) - \frac{h^2}{2}\frac{\partial}{\partial z}\left(\frac{1}{m_z^*(y,z)}\frac{\partial}{\partial z}\right) + U(x,y,z) \quad (2)$$

Here m_x^*, m_y^* and m_z^* are the electron effective mass in the x, y, and z directions, respectively, and $U(x, y, z)$ is the electron conduction band-edge profile in the active device. After the device Hamiltonian H is obtained, we can calculate the electron density and current using the NEGF approach. The NEGF approach is a widely used method for the simulation of nanoscale electronic devices. Here we list the relevant equations for our particular case. The retarded Green's function of the active device is defined as

$$G(E) = [ES - H - \Sigma_s(E) - \Sigma_1(E) - \Sigma_2(E)]^{-1} \quad (3)$$

Where $\sum_S$ is the self-energy that accounts for the scattering inside the device (zero in the case of ballistic approach), and $\sum_1$ ($\sum_2$) is the self-energy caused by coupling between device and the source (drain) [7].

3.2. Uncoupled Mode Space Approach

The uncoupled mode space approach treats quantum confinement and transport separately. In the simulation of NWTs, we assume that the shape of the Si body is uniform along the x direction. As a result, the confinement potential profile (in the y-z plane) varies very slowly along the channel direction.

For instance, the conduction band-edge $U(x, y, z)$ takes the same shape but different values at different x. For this reason, the eigen functions $\xi^m(y, z; x)$ are 10 approximately the same along the channel although the eigen values $E_{sub}^m(x)$ is different. So we assume

$$\xi^m(y, z; x) = \xi^m(y, z) \quad (4)$$

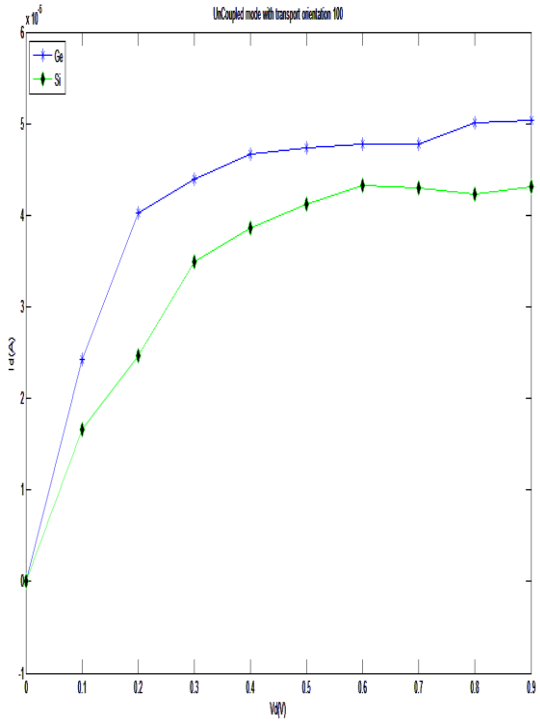
The retarded Green's function for mode m of the active device is defined as [7]

$$G^m(E) = [ES^m - h_{mm} - \Sigma_s^m(E) - \Sigma_1^m(E) - \Sigma_2^m(E)]^{-1} \quad (5)$$

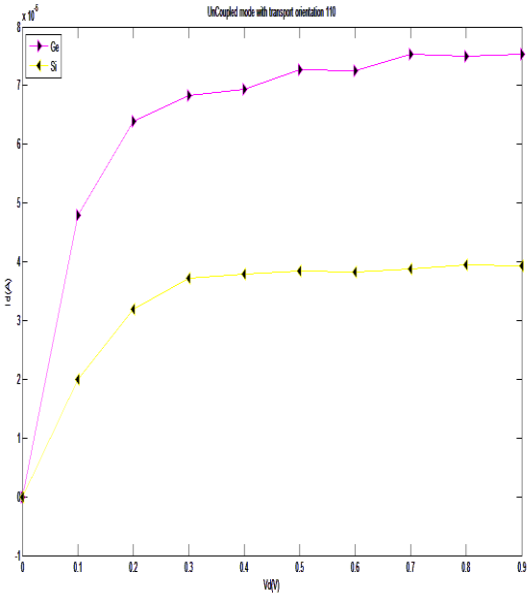
4. Simulation and Discussion

In this work, the mode space (coupled/uncoupled) NEGF transport is considered. We include the phonon scattering in the tool, thus computation complexity increases thus lead to a much longer simulation time. Although silicon is the most common and economical material used in semiconductor industry, it has some limitations and maybe reaches its physical end soon. There are some other materials which are very active in research and exhibit some promising improvement over silicon. Hence we compare the silicon and germanium semiconductor for the nanowire transistor channel material. The gate work function of 4.15eV is used, which is for the metal aluminium. The nanowire diameter is considered to be 5nm, oxide thickness of SiO_2 is 1nm, gate length is of 10nm and the source drain extension length is of 8nm each. The doping profile of 2×10^{20} /cm^3 is considered for the source drain extensions. The channel region doping has been set to zero which provides results similar to that of an intrinsic channel.

The gate voltage is varied from 400 mV to 700 mV and the drain current is extracted for different drain bias by using silicon as the channel material with coupled/uncoupled mode space approach. The same is repeated by using germanium as the channel material. It is inferred from the figure 2(a, b, c) and 3(a, b, c) that the nanowire transistor germanium as channel material has more ON current and they show excellent output characteristics when compared with that of the silicon counterpart for various crystal orientation (100,110,111) with coupled/uncoupled model transport.



a



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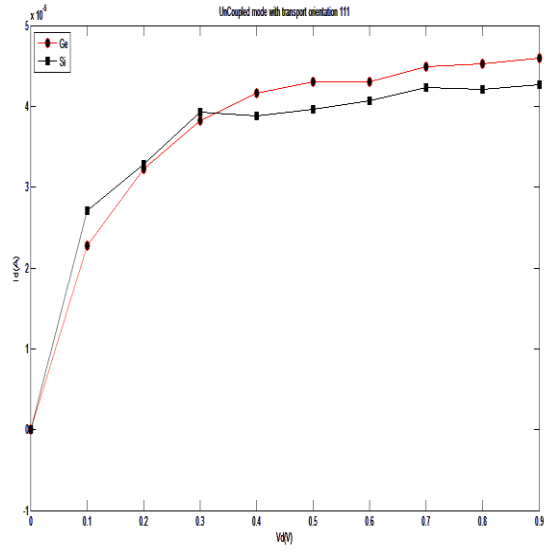
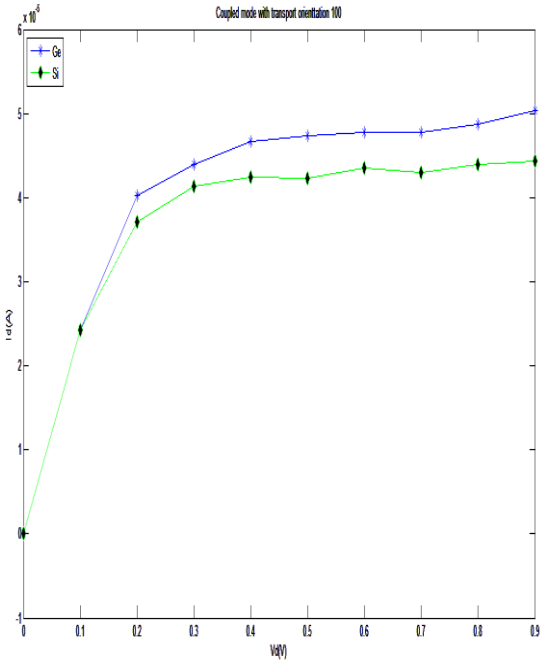
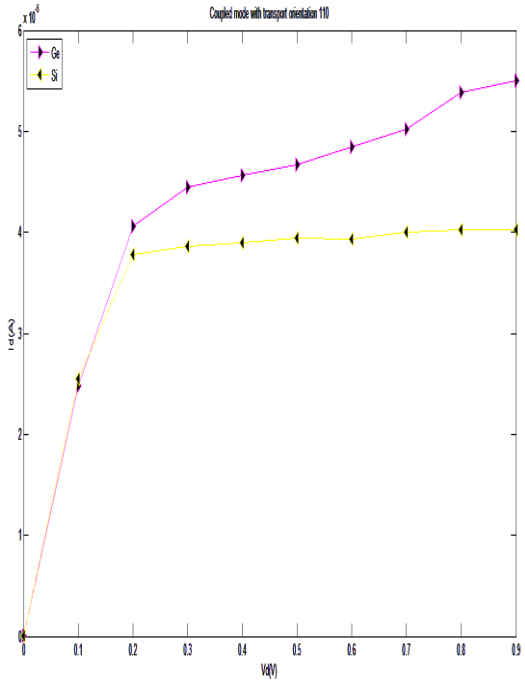


c

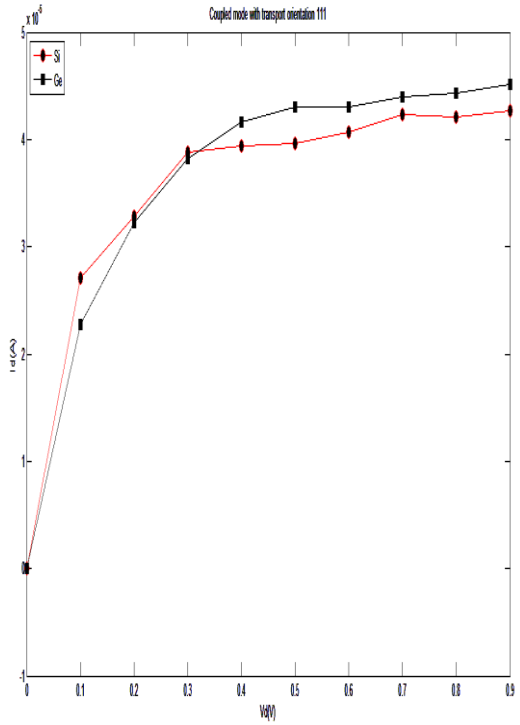


a



b

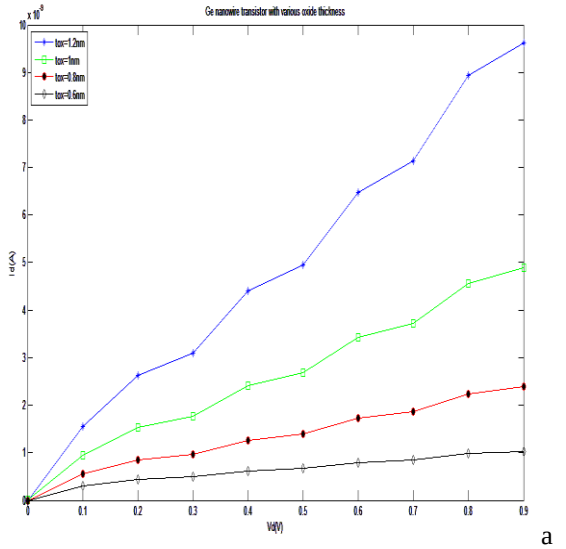
Fig. 1: Plot of drain current (y axis)versus drain voltage (x axis) of Silicon and Germanium nanowire transistor withUncoupled mode space approach for various crystal orientations (a) crystal orientation 100 (b) crystal orientation 110 (c) crystal orientation 111.



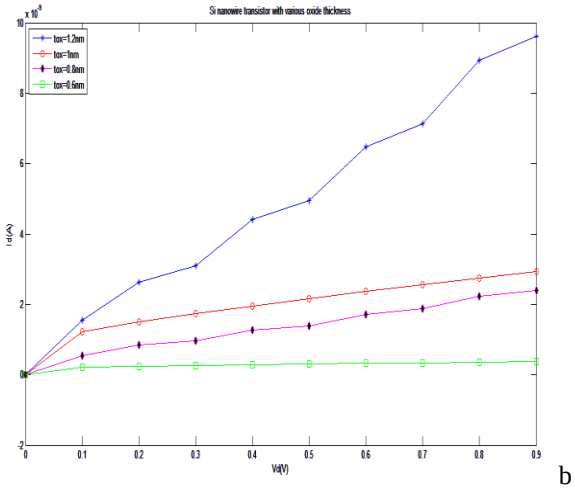
c

Fig. 2: Plot of drain current (y axis) versus drain voltage (x axis) of Silicon and Germanium nanowire transistor with Coupled mode space approach for various crystal orientations (a) crystal orientation 100 (b) crystal orientation 110 (c) crystal orientation 111.

From the analysis of the silicon and germanium NWTs, the orientation of (100 and 111) had less ON current compared with orientation of (110). And also for different orientation of mode space approach germanium NWTs give better performance than silicon NWTs. From this we got a conclusion that germanium NWTs have higher mobility than silicon NWTs.



a



b

Fig. 3: Plot of drain current (y axis) versus drain voltage (x axis) for various gate bias for various values of oxide thickness (a) Germanium nanowire transitor (b) Silicon nanowire transistor.

Figure 3(a) and 3(b) shows that the oxide thickness of material get decreased the ON current of the nanowire transistor also degrades. Eventhough germanium NWTs had higher mobility, for narrow downing the device size in nanometers range got lesser performance.Inorder to over come from this, we would move onto high-K valued materials for making nanowire transistors.

5. Conclusion

The simulation study reveals that the germanium nanowire transistor is an attractive candidate for CMOS device design for future technology nodes. Nanowire transistors build using germanium material is providing high I_{ON} current than the silicon based nanowire transistor, thus future CMOS devices will be aiming at higher device drive current and faster operation speed. However, at this time the nanowire transistor still is in its early stage, there is a lot of room to optimize the structure parameters and lots of new phenomenon to be explored by both experimental and computational approach.

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