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Design and Development of a High Speed Pipelined-Cyclic ADC with 1.5 bits/Stage Error Correction

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Abstract

The paper describes an improved architecture of an 8-bit Analog to Digital Converter (ADC) based upon both the traditional Pipeline and the Cyclic ADC architectures. Cyclic ADC has a very low component count but the flip side is that it has a very low speed. On the other hand, a pipeline ADC has a comparatively higher speed but needs more number of components than a Cyclic ADC - the component count depends on both the resolution and the number of bits per stage. The proposed design incorporates the advantageous features of both types to realize a pipelined cyclic ADC. It is higher in speed than the cyclic ADC and its component count is much less than a conventional pipeline ADC. Hence the space and power requirements are also reduced.

The proposed design has a high throughput because in each clock cycle a new set of data is made available from its eight output pins, while its latency is a maximum of one primary clock cycle only. Since the accuracy of both pipeline and cyclic ADCs are moderate, hence the 1.5 bits/stage error correction logic is used to increase their accuracy. The proposed design also incorporates the same error correction logic to get error free output bits. It is simulated in MATLAB SIMULINK environment which establishes the validity of the proposed design.

Keywords

Pipeline ADC, Cyclic ADC, 1.5 bits/stage, Digital Error Correction, MATLAB Simulink.

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1. Introduction

Analog to Digital Converters or simply ADCs are very important in modern systems which need the integration of analog signals with digital systems. These may be recording of music to communication to medical instrumentation. There are many types of ADCs available in the market having different architectures, sizes, speed and accuracy – depending on the specific application requirements.

The demand for smaller, faster, lower power and accurate converters has led to the investigation of alternative ADC design techniques **[1][2]**. There are a number of designs available on the basis of architecture and performance. Among them the flash ADC is the fastest one. But it needs 2^n-1 comparators **[3]** for n-bit resolution. It is not used for higher resolution because of exponential rise in the number of comparators. Thus higher resolution flash ADCs are not normally available in the market. This, coupled with inherent comparator errors, limits its usage **[4]**. To overcome these drawbacks, pipeline ADC came into the market to replace flash ADCs. Pipeline ADC is fast and of medium accuracy **[5]**. The term 'Pipeline' refers to stage by stage processing **[6]**. A pipeline ADC consists of a number of stages based on low resolution flash ADCs. It employs binary search for analog value. In each stage it performs the same operations, i.e. input quantization, regain analog voltage by DAC, subtract the DAC output from the held input and amplify the residue. Pipeline ADCs normally have a higher conversion rate and higher resolution compared to other ADCs **[7].** But it is somewhat slower than a flash ADC. It fits perfectly when we need higher resolution with moderate speed **[8]**. Use of digital error correction can increase its accuracy. For error correction, 1.5 bits/stage method is used. It is the most advanced error correction technique for pipeline ADCs to overcome comparator offset and nonlinearity error **[9]**. Thus, this is the simplest possible correction scheme, and cannot be improved any further **[10]**.

Cyclic ADCs depend for their operation on the feedback of the residue again and again to generate the desired digital output. Accuracy of cyclic ADCs

depend entirely on the components **[11]**. Accuracy of cyclic ADCs may seriously be affected if the offset error present in the comparator is not taken care of. Since the same comparator is repetitively used to get the output bits, it will have a much more degrading effect on the accuracy of such ADCs. Since it consists of just one stage, it is simple in nature, consumes less power and space, cost effective and has a low component count but very slow in speed.

The proposed architecture incorporates the design features of both pipeline and cyclic ADCs for its realization.

The accuracy requirement for pipeline ADCs is very important. The ADC in the first stage must be the most accurate **[10]**. There are few error correction techniques available for pipeline ADCs **[1][4][8-13]**. Among them Digital Redundancy and Error Correction technique, typically known as 1.5 bits/stage, is the most simple and effective one **[10]**. 1.5 bits per stage is basically 1 bit per stage to which 0.5 redundancy is added to handle device tolerances and imperfections **[13]**. The previous digital error correction techniques employed three possible ways to take care of comparator offsets i.e. add, subtract or do nothing, which made these techniques quite complex to implement. They also add to more component count. The error correction technique proposed by S H Lewis has overcome this problem by introducing redundancy by making the sum of resolutions greater than the total resolution. By eliminating redundancy using a simple Overlap and Add scheme, the effect of offset and nonlinearity can be eliminated **[9]**.

The transfer characteristics of a 2 bits/stage design is shown in **Figure 1**.

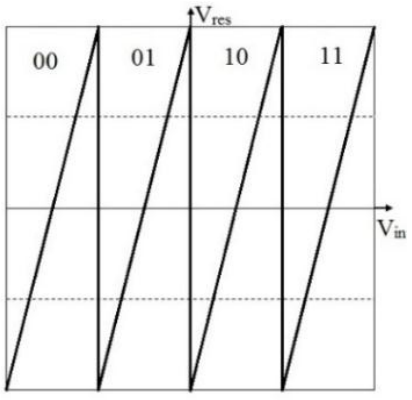

Figure 1.Transfer curve of a 2 bit ADC

Any offset (both positive and negative) present in a comparator can lead to the residue transfer curve go out of range as shown in **Figure 2**.

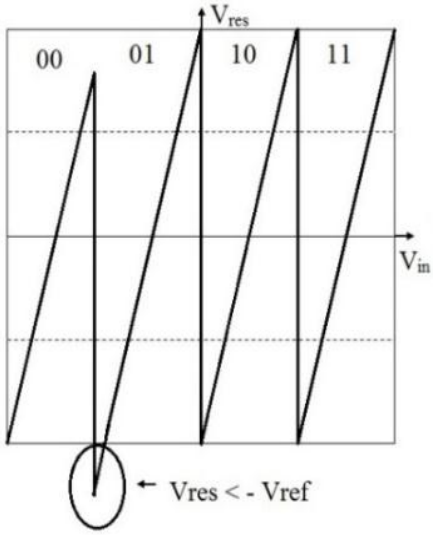

Figure 2. Out of range error

To overcome the problem, the gain is reduced to half so that the residue will not go out of range as shown in **Figure 3**.

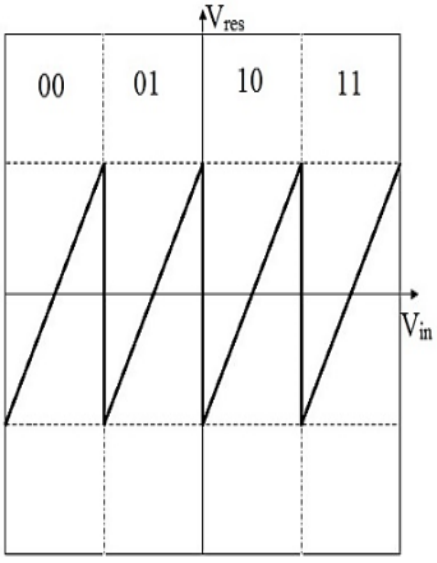

Figure 3. Transfer curve with reduced gain

It is assumed that the offset is strictly bounded to $\pm\frac{1}{2}$ LSB. Now in the next step an offset of $+\frac{1}{2}$ LSB is intentionally added so that if any offset error exists in

any comparator, it will stay in the same voltage range. This approach makes the last bit pair, i.e. 11 redundant. As a result, after this transformation the residue transfer curve looks like as in **Figure 4.**

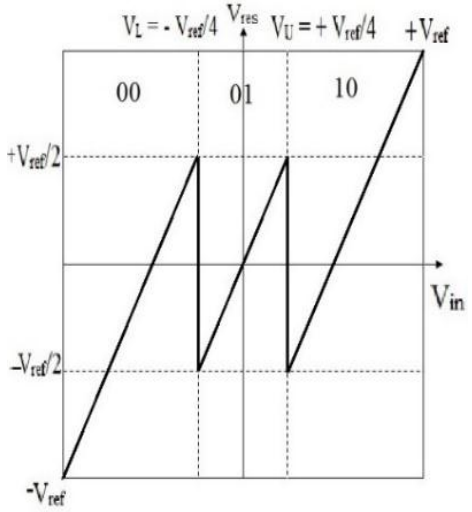

Figure 4. Transfer curve for 1.5 bits/stage

Now the SADC has only two decision levels, i.e. $+\frac{1}{4}V_{ref}$ and $-\frac{1}{4}V_{ref}$. These comparison voltages are named as V_U and V_L. A $+\frac{1}{2}$ LSB offset is also added to the SDAC. **Table 1** shows the working principle of a stage **[14]**.

Table 1. Working principle of a 1.5 bit/stage

Input Voltage	Input Range	ADC Output		DAC Output	Residue
		B_1	B_0		
$V_{in}<V_L$	Low	0	0	$-V_{ref}$	$2V_{in}+V_{ref}$
$V_L<V_{in}<V_U$	Medium	0	1	0	$2V_{in}$
$V_{in}>V_U$	High	1	0	$+V_{ref}$	$2V_{in}-V_{ref}$

Redundancy can be eliminated by a simple Overlap and Add scheme described below. After digital error correction, output digital bits are free from comparator offset and nonlinearity.

$$
\begin{array}{cccccccc}
B_{11} & B_{01} & & & & & & \\
 & B_{12} & B_{02} & & & & & \\
 & & B_{13} & B_{03} & & & & \\
 & & & B_{14} & B_{04} & & & \\
 & & & & \ldots. & \ldots. & & \\
 & & & & & & B_{1m} & B_{0m} \\
\hline
B_0 & B_1 & B_2 & B_3 & \ldots\ldots & B_{m-1} & B_m &
\end{array}
$$

Since in this case the number of input voltage ranges is 3, therefore the resolution is $\log_2 3 \approx 1.5$ bit **[9]**. Thus, the design is termed 1.5 bits/stage.

2. Circuit Description and Working Principle

Figure 5 shows the block diagram of the proposed 8 bit Pipelined-Cyclic ADC, working in the range of +5V to -5V. The circuit consists of two switches (Block 1 and Block 5), two sample and holds i.e. S/Hs (Block 2 and Block 6), four Stages (Block 3, 4, 7 and 8), bit shift and storage block (Block 9) and digital error correction block (Block 10). The two switches operate at a frequency *f* while the two S/Hs operate at 2*f*. Each stage consists of a Sub-ADC (SADC), a Sub-DAC (SDAC), a gain amplifier and a comparator. The design (Block 1 to Block 8) is divided into two equal parts i.e. Part 1 and Part 2. These two parts are connected according to pipelined architecture. Each stage is responsible for 1.5 bits digital output. The timing diagram for proper operation of the proposed 8-bit pipelined-cyclic ADC is shown in **Figure 6**.

It is assumed that all the F/Fs etc. are positive edge triggered and initially they are resetted. Switch 1accepts V_{in} and switch 2 accepts the output from stage 2 at the beginning of each T_P (each primary clock pulse) while the feedback residues are accepted by switches 1 and 2 at the middle of each T_P.

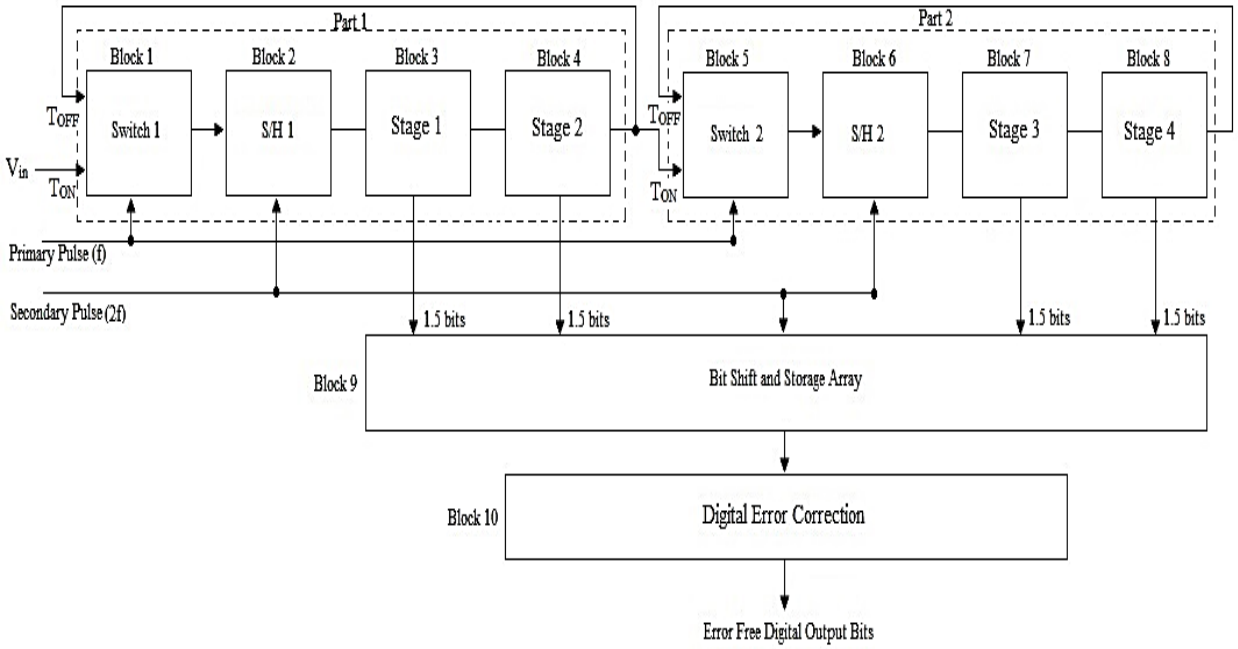

Figure 5. Block diagram of the proposed circuit

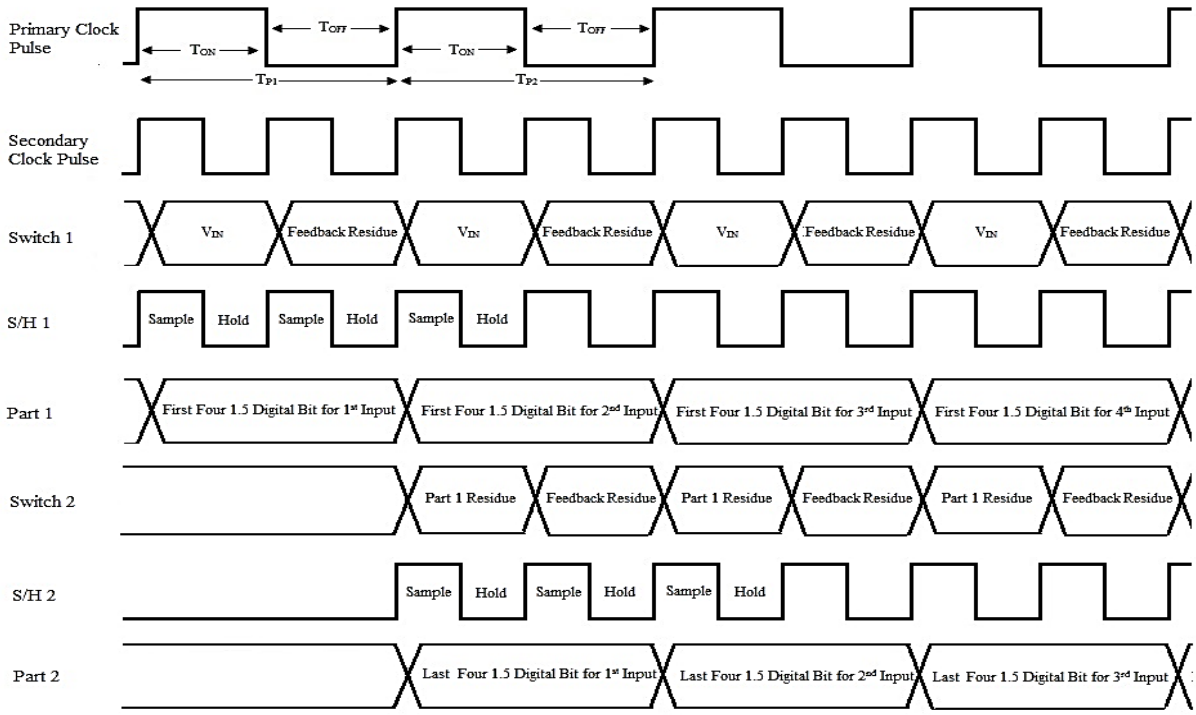

Figure 6. Timing diagram

At start when Switch 1 (Block 1) is triggered with primary clock pulse, it allows V_{in} for T_{ON} time period. S/H1 (Block 2) samples V_{in} and holds the same until the next positive edge comes. As per the circuit design, since S/H1 (and for that matter S/H2 also) operate at 2*f* frequency, it gets the next low to high transition at 50% of $T_{P.}$ Stage 1 (Block 3) receives the output of S/H1 and **Figure 7** represents the MATLAB circuit diagram of any one stage.

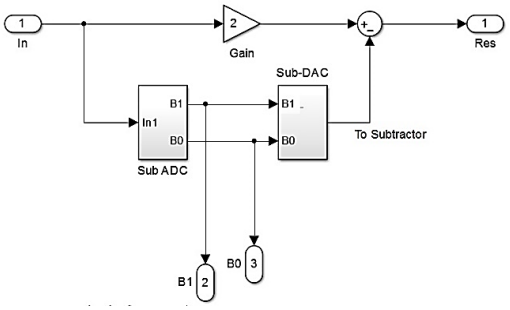

Figure 7. MATLAB circuit diagram of a stage

There are two comparators in a SADC, which compare the input signal with two comparison voltage levels i.e.

$$V_U = \frac{+V_{ref}}{4} = \frac{+5}{4}V = +1.25V$$

$$V_L = \frac{-V_{ref}}{4} = \frac{-5}{4}V = -1.25V$$

and produces 1.5 bit digital output bits B_1 B_0. It is shown in **Figure 8**.

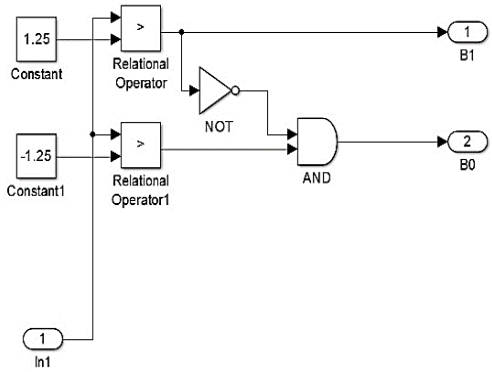

Figure 8. MATLAB circuit of SADC

SDAC produces an analog output according to the produced digital output of SADC. The MATLAB circuit of SDAC is shown in **Figure 9**.

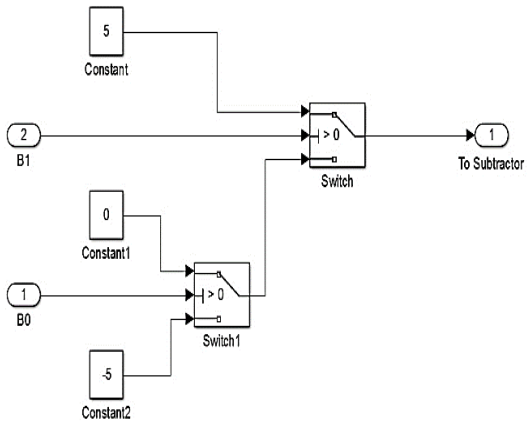

Figure 9. MATLAB circuit of SDAC

Subtractor subtracts the SDAC output from the amplified input and generates a residue.The produced residue of stage 1 is the input to stage 2. Stage 2 also produces 1.5 bit digital output and a residue. The whole process is completed within T_{ON} period of the primary clock pulse.

At the beginning of T_{OFF} state, switch 1 (Block 1) allows the feedback residue (and simultaneously blocking V_{in}) as input from stage 2 (Block 4). S/H1 (Block 2) samples this input. At the same time, switch 2 allows feedback residue as input from stage 4. So the residue from Part 1 cannot go to the Part 2. As described earlier for stage 1, stage 2 also produces two 1.5 bit digital outputs and a residue.

At the T_{ON} state of T_{P2}, switch 2 (Block 5) gets the residue from the stage 2 (Block 4). Since Part 2 is similar to Part 1, thus in period $T_{P2,}$ Part 2 also produces four 1.5 digital output bits. As a result after two primary clock pulses, eight 1.5 digital bits are obtained which correspond to the same V_{in}. During T_{ON} of $T_{P2,}$ Part 1 takes in a new input and produces four 1.5 bit digital outputs during this time. The whole process is repeated for every primary clock cycle.

These bits are stored in Bit Shift and Storage Block (Block 9). This block is nothing but a SIPO (Serial Input Parallel Output) array. SIPOs are triggered from the secondary clock, having a frequency 2*f*. After Digital Error Correction i.e. a simple overlap and addition, 8 error free bits in each primary cycle is obtained.

3. Simulation of 8 bit Design

Figure 10 is the actual circuit to realize the proposed 8 bit design that has been simulated in MATLAB SIMULINK environment. The design was simulated for various kinds of input signals having varied frequencies, both with and without any added offset voltage. The digital outputs were reconstructed via DAC for each case and compared with the actual input signal.

The input-output characteristics for the various cases were studied. **Table 2** shows the simulated results for the input voltages and corresponding reconstructed output voltages for a perfect ADC, proposed design without added offset and with added offset. **Figures 11a, 11b** and **11c** represent respectively analog input voltages and the corresponding output voltages for a perfect ADC, for the proposed ADC without any added offset and lastly for the proposed ADC with added offset. The nature of the three plots suggests that there is no noticeable deviation amongst them even when sufficient offset is added.

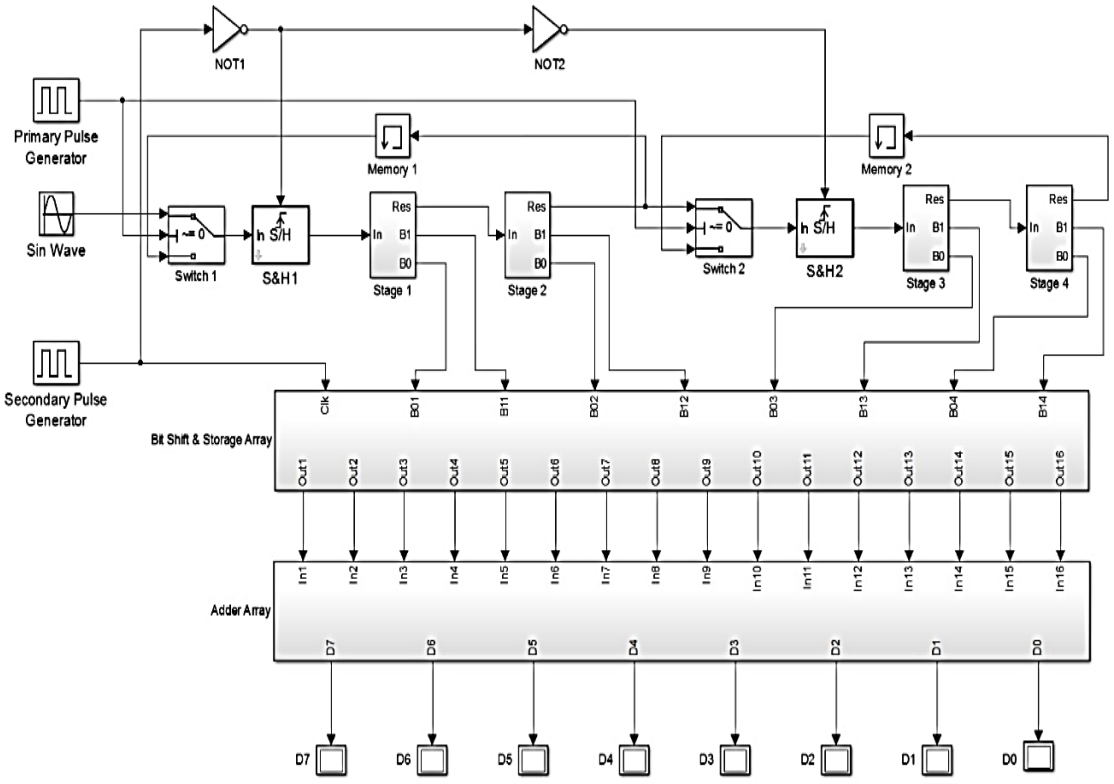

Figure 10. Simulated circuit in MATLAB

Table 2: Experimental results of 8 bit ADC

V_{in} in Volt	Equivalent Digital Output								V^1_{out} in Volt	V^2_{out} in Volt	V^3_{out} in Volt
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0			
-5.00	0	0	0	0	0	0	0	0	-5.000	-5.000	-5.000
-4.50	0	0	0	0	1	1	0	1	-4.490	-4.490	-4.529
-4.00	0	0	0	1	1	0	1	0	-3.980	-4.019	-4.020
-3.50	0	0	1	0	0	1	1	0	-3.510	-3.510	-3.510
-3.00	0	0	1	1	0	0	1	1	-3.000	-3.000	-3.000
-2.50	0	1	0	0	0	0	0	0	-2.490	-2.490	-2.490
-2.00	0	1	0	0	1	1	0	1	-1.980	-1.980	-2.020
-1.50	0	1	0	1	1	0	1	0	-1.471	-1.510	-1.510

V_{in} in Volt	Equivalent Digital Output								V^1_{out} in Volt	V^2_{out} in Volt	V^3_{out} in Volt
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0			
-1.25	0	1	1	0	0	0	0	0	-1.235	-1.235	-1.235
-1.00	0	1	1	0	0	1	1	0	-1.000	-1.000	-1.000
-0.75	0	1	1	0	1	1	0	1	-0.726	-0.7647	-0.7647
-0.50	0	1	1	1	0	0	1	1	-0.490	-0.4902	-0.4902
-0.25	0	1	1	1	1	0	1	0	-0.216	-0.2549	-0.2549
0.00	1	0	0	0	0	0	0	0	0.019	0.019	0.0196
0.25	1	0	0	0	0	1	1	0	0.255	0.255	0.2549
0.50	1	0	0	0	1	1	0	1	0.529	0.529	0.4902
0.75	1	0	0	1	0	0	1	1	0.765	0.765	0.7647
1.00	1	0	0	1	1	0	1	0	1.039	1.000	1
1.25	1	0	1	0	0	0	0	0	1.274	1.275	1.275
1.50	1	0	1	0	0	1	1	0	1.510	1.510	1.510
2.00	1	0	1	1	0	0	1	1	2.020	2.020	2.020
2.50	1	1	0	0	0	0	0	0	2.529	2.529	2.529
3.00	1	1	0	0	1	1	0	1	3.039	3.039	3.000
3.50	1	1	0	1	1	0	1	0	3.549	3.510	3.510
4.00	1	1	1	0	0	1	1	0	4.019	4.02	4.020
4.50	1	1	1	1	0	0	1	1	4.529	4.529	4.529
5.00	1	1	1	1	1	1	1	1	5.000	5.000	5.000

where,
V_{in} = Input analog voltage
V^1_{out} = Reconstructed output voltage for a perfect 8 bit ADC
V^2_{out} = Reconstructed output voltage for the proposed 8 bit ADC without added offset
V^3_{out} = Reconstructed output voltage for the proposed 8 bit ADC with added offset

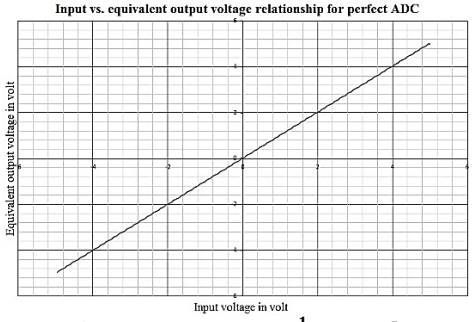

Figure 11a: V_{in} vs. V^1_{out} graph

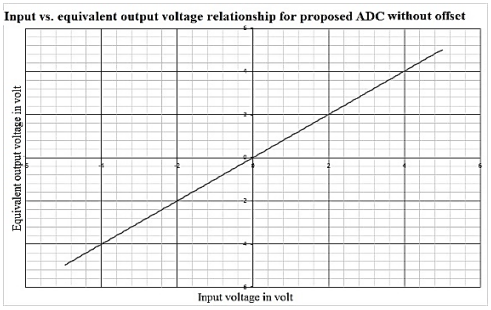

Figure 11b: V_{in} vs. V^2_{out} graph

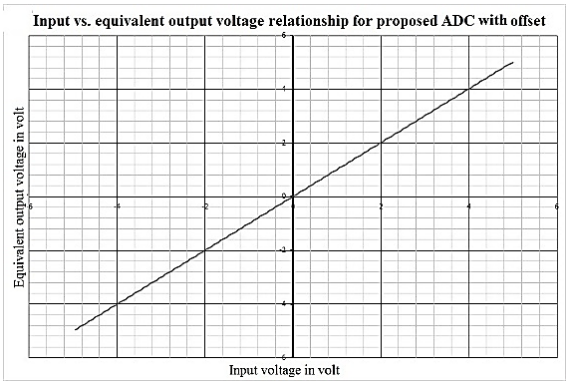

Figure 11c: V_{in} vs. V^3_{out} graph

Table 3 shows the calculated % errors for all three cases respectively. Formula of calculating the % error is calculated as per **Equation 1**.

$$\% \; Error = \frac{(V_{in} - V^i_{out})}{V_{in}} \times 100\% \qquad (1)$$

Where,
V_{in} is the actual analog input voltage,
V^i_{out} is the equivalent output analog voltage.
for perfect ADC (i = 1)
proposed ADC without any added offset (i = 2)
proposed ADC with any added offset (i = 3)

Table 3: Table for input vs. corresponding percentage error for three cases.

V_{in} in Volt	% Error of V^1_{out} (E_1)	% Error of V^2_{out} (E_2)	% Error of V^3_{out} (E_3)
-5.00	0	0	0
-4.75	-0.31579	-0.29474	-0.31579
-4.50	0.222222	0.222222	-0.64444
-4.25	-0.11765	-0.09412	-0.11765
-4.00	0.5	-0.475	-0.5
-3.75	0.133333	0.133333	0.133333
-3.50	-0.28571	-0.28571	-0.28571
-3.25	0.461538	0.461538	-0.76923
-3.00	0	0	0
-2.75	0.872727	-0.54545	-0.54545
-2.50	0.4	0.4	0.4
-2.25	-0.22222	-0.22222	-0.22222
-2.00	1	1	-1
-1.75	0.285714	0.285714	0.285714
-1.50	1.933333	-0.66667	-0.66667
-1.25	1.2	1.2	1.2
-1.00	0	0	0
-0.75	3.2	2	-1.96
-0.50	2	2	1.96
-0.25	13.6	-2	-1.96
0.00	#DIV/0!	#DIV/0!	#DIV/0!
0.25	-2	-2	-1.96
0.50	-5.8	-5.8	1.96
0.75	-2	-2	-1.96
1.00	-3.9	0	0
1.25	-1.92	-2	-2
1.50	-0.66667	-0.66667	-0.66667
1.75	-1.94286	-1.94286	0.285714
2.00	-1	-1	-1
2.25	-1.95556	-0.22222	-0.22222
2.50	-1.16	-1.16	-1.16
2.75	-0.21818	-0.54545	-0.54545
3.00	-1.3	-1.3	0
3.25	-0.73846	-0.76923	-0.76923
3.50	-1.4	-0.28571	-0.28571
3.75	-0.90667	-0.90667	-0.90667
4.00	-0.475	-0.5	-0.5
4.25	-1.03529	-1.03529	-0.11765
4.50	-0.64444	-0.64444	-0.64444
4.75	-1.13684	-0.31579	-0.31579
5.00	0	0	0

Input voltage vs. corresponding % error graphs are shown in **Figure 12a, 12b** and **12c** respectively.

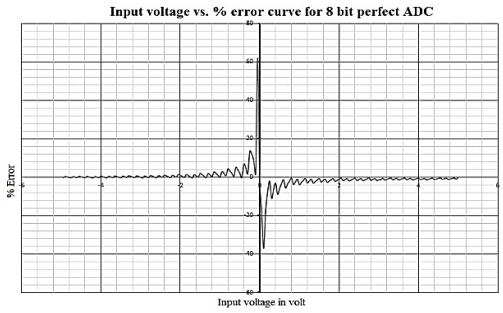

Figure 12a: V_{in} vs. E_1 graph

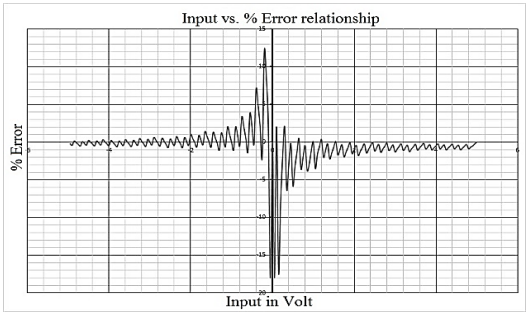

Figure 12b: V_{in} vs. E_2 graph

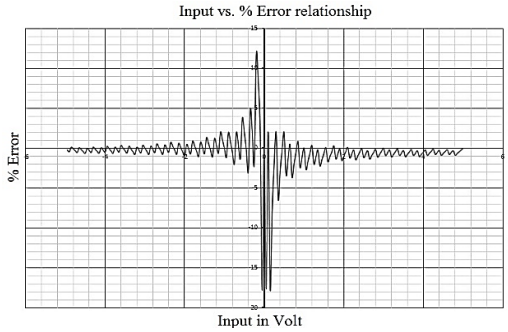

Figure 12c: V_{in} vs. E_3 graph

From these figures it can be seen that the percentage error lies under 2-3% for most of the range. There is a sharp rise in the value of the percentage error for analog voltages at around zero, which is only to be expected. Since 1.5 bits per stage is applied in the proposed design, no discernable change is perceptible between these graphs.

Figure 13 shows the simulated result for an arbitrary function and its reconstructed version for two cases – without and with offset. It is seen that the reconstructed signal faithfully follows the input signal and the effect of offset is nullified very efficiently because of application of 1.5 bits per stage algorithm.

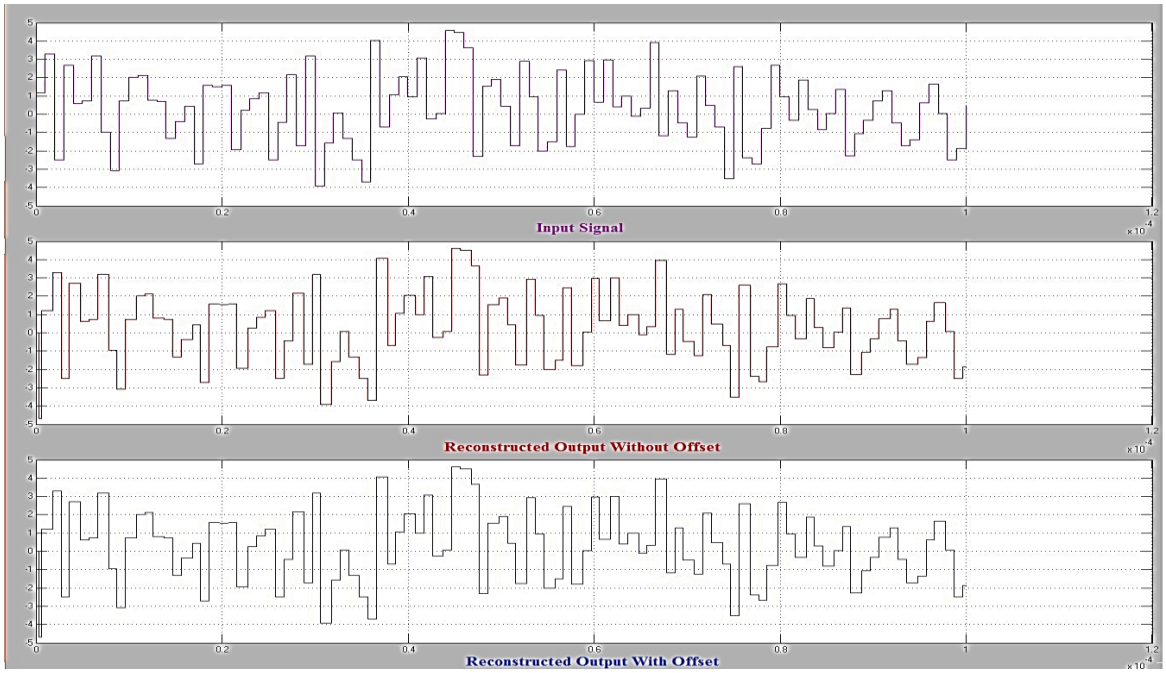

Figure 13: Simulated waveform with arbitrary wave

4. Conclusion and Future Work

The designed circuit outputs eight digital bits in every primary clock cycle. It has a latency of one cycle only. A conventional 8 bit pipeline ADC with 1.5 bits per stage has identical throughput as the designed one but has a latency of seven cycles. Thus the proposed pipelined cyclic ADC can be faster than both the conventional pipeline and cyclic ADC. However, its component count is higher than a cyclic ADC but much less than a conventional pipeline ADC as a pipeline ADC would need 8 stages to realize an 8 bit design with a 1.5 bits/stage. Thus both speed wise and component count wise, the designed circuit is a better proposition than the other two–referencing to same accuracy level of both. Due to application of 1.5 bits/stage error correction method, the proposed design is free from any offset error. A 16 bit ADC of the designed type would have a latency of only three clock cycles while it is fifteen for a cyclic ADC and a conventional pipeline ADC having a stage resolution of 1.5 bits per stage.

The future work of this project includes design and simulation of the proposed model using Xilinx and also in hardware, study its performance characteristics and compare with other ADCs available in market.

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