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Comparison of Conventional 6T SRAM cell and FinFET based 6T SRAM Cell Parameters at 45nm Technology

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Abstract

When working for low power application the main estimation is to reduce leakage components and parameters. This stanza explores a vast link towards low leakage power SRAM cells using new technology and devices. The RAM contains bi-stable cross coupled latch which has V_th higher in write mode access MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and lower V_th in read access mode MOSFET which is preferred for low leakage current and power without any distortion. The most promising substitute which are replacing bulk CMOS is DELTA (fully Depleted Lean channel Transistor) or FinFET (Fin-shaped field-effect transistor). For better performance and lower leakage parameters we can use FinFET either be shorted gates or independent gates. DELTA gates has good Short Channel Effects (SCE's) compared to conventional based CMOS. Static Random Access Memory (SRAM) plays a most significant role in the microprocessor world, but as the technology is scaled down in nanometers, leakage current, leakage power and delay are the most common problems for SRAM cell which is basically designed in low power application. About 40-50% of the total power of the SRAM cell is dissipated due to the leakage occurs from the transistor. In this paper we compare the performance parameters of conventional 6T SRAM cell with FinFET based 6T SRAM cell. And determines that during write operation of FinFET based 6T SRAM cell gives leakage current is 69pA, leakage power is 7.581nW and delay is 20.55ns and for read operation of leakage current is 53.90pA, leakage power is 1.709µW and delay is 21.44ns.

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Keywords

SRAM, FinFET, DELTA, Short Channel Effects, Leakage Current, Leakage Power, Delay.

1. Introduction

As we moved down into a previous scenario of SRAM progress, we see that CMOS technology has been scaled down to achieve higher performer larger memory capacity and low power consumption [1]. Static Random Access Memory has its own applications mainly in the various types of portable devices. Now days, the larger portion of the total chip area covered by SRAM plays a vital role in microprocessors design. As per the today's scenario, we need a several transistors implemented on a single chip which is comparatively smaller than the previous design implementation. As the size is reduced the effect of leakage current, leakage power is increased in the circuit [2].

Multiple gate devices for 45nm technology node are FinFET, ΩFET, cylindrical FET [3]. A critical Emerging Research Devices (ERD) to improve interconnects, connects, control embedded interface, thermo-dynamic stability and limit this phenomena [4]. All this effects and phenomena improvement is noticed in International Technology Roadmap for semiconductor (ITRS) research issue table of ERD in 2013 [5]. Now a day, research in VLSI domain facing tremendous problem to achieve this technological challenges associated with double gate transistors [6]. In double gate, I_{DD} drain current (drive) is two times than single gate transistor then the gate capacitance also double in double gate. The intrinsic propagation delay is simply:

$$C_g \frac{V_{DD}}{I_{DD}} \quad (1)$$

But, for double gate the intrinsic propagation delay comes with the factor square of V_{DD} [7].
The intrinsic propagation delay is:

$$C_g {V_{DD}}^2 \quad (2)$$

If the same width is applied then the supply voltage of double gate FET becomes two times lower than the single gate of FET. That's the reason MuGFET is preferred over single gate [8].

2. FinFET

FinFET is a Device which have "fin" similar to the fish that is it have Source and Drain as a fin on either side of the Gate and it is appear as a "fin". It is first introduced by Berkeley researchers of University of California and described the FinFET as a Non-Planer, Independent Gate transistor built on an SOI (Silicon on Insulator) based on single Gate structure.

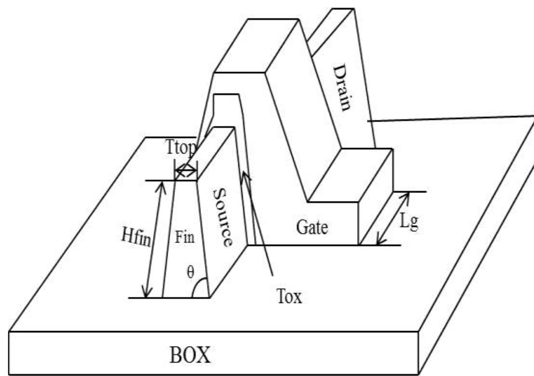

Figure 1:FinFET [9]

As we stated before that FinFET has "fin" like structure is clearly shown in the above figure. Here H_{fin} is the height of the Silicon fin, L_g is the physical Gate Length of the FinFET, T_{top} is the thickness of the silicon fin and T_{ox} is the thickness of Gate Oxide. In single gate devices as the channel length reach a specific value and after that if we reduce the channel length the short channel effect come into play and the performance of the device start degrading due to the short channel effect. This is the major drawback of the single gate devices. To overcome the Short Channel Effect First Double Gate FinFET is introduce which successful reduce the Short Channel Effect but it required double power supply for both the Gate. Than Short Gate FinFET is introduce which show great reduction on Short Channel Effect and also require single power supply.

1. Drain Curent of FinFET

$$I_D = \frac{W_{eff}}{L_{eff}} B(V_{GS} - V_{th})^m \quad (3)$$

$$I_D = I_{Dsat}\left(2 - \frac{V_{DS}}{V_{Dsat}}\right)\frac{V_{DS}}{V_{DSAT}} \quad (4)$$

When $V_{DS} < V_{Dsat}$: Linear Region

$$I_d = 0 \quad (5)$$

When $V_{GS} < V_{th}$: Cutoff Region

Above equation show the Drain current in different Region that is Linear Region, Saturation Region and Cut-off Region of FinFET Transistor.

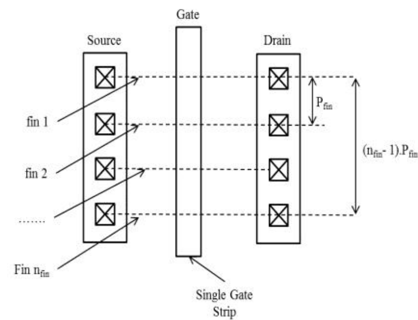

Figure 2:Layout of Single Gate FinFET[9]

Figure 2 shows an SG-mode FinFET in which four fins have been connected in parallel. The width of this device is 4Wmin. The area occupied by this device is proportional to $(n_{fin} - 1)P_{fin}$, where $P_{fin}$is the fin pitch defined by the process technology.

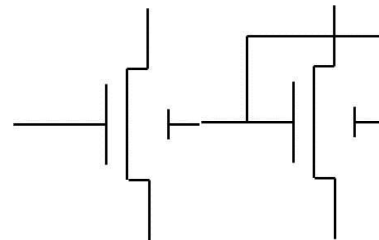

Figure 3: Independent Gate amd Short Gate FinFET

FinFET is further classified into two types Short Gate FinFET and Independent Gate FinFET. FinFET has very good Electrostatic control of the channel that is it has full control over channel and boasts a near-ideal sub-threshold behavior (associated with leakage), it is not achieved in planner device without

considerable effort. FinFET greatly reduce short channel effort, which in planer technology are very complex and have a sufficient impact on gate length variation and on electrical performance. FinFET has higher integration density and smaller variability.

Multiple gates have many advantages and disadvantages. To reduce disadvantages we are examine SRAM cell using (DG) FinFET [10] in this paper and studied improvement in leakage power and currents consumption using Multi threshold CMOS compared to the results with SRAM based on (DG) FinFET. FinFET has two broad divisions in SOI and bulk FinFET. Short channel effect and high doping cons. Found in bulk FinFET compare to SOI FinFET [11]-[12].

So, FinFET on silicon on insulator is preferred over bulk FinFET [13].Double gate MOSFET and MuGFET are floating body devices into which charge trapping occurs in body this causes leakage due to radiation. Charge trapping occurs due to 'back channel interface' and 'total dose latch effect' [14]. Trapping in buried oxide potential of body modulates, when depletion between source and body is lower than electrons injected into the body and drain region collect it [15]. If electric field is high to cause impact ionization in drain occur and lead to current runaway causing snapback [16].

3. SRAM Cell

Six transistors are used to made single bit 6T SRAM cell in which two nMOS are used for bit line control transistors or pass transistors (N3 & N4) and to form cross-coupled inverters four transistors used, that are two pMOS (P1 & P2) and two nMOS (N1 & N2) [17]. Bi-stable latch means two inverters are connected back to back.

Two nMOS (N3 & N4) are access transistor to write on latch by write line on gate terminals and drain out the data from bit line to latch. Read and write operations are performed by using two bit lines [18]. The operation of SRAM is in three modes: write mode, hold mode and read mode. The sequence of modes are first data is write by using bit line next the hold mode holds the write data in cross coupled latch and after that when data required to read then sense amplifier sense the data. The schematic diagram of 6T SRAM Cell is shown in Figure.1

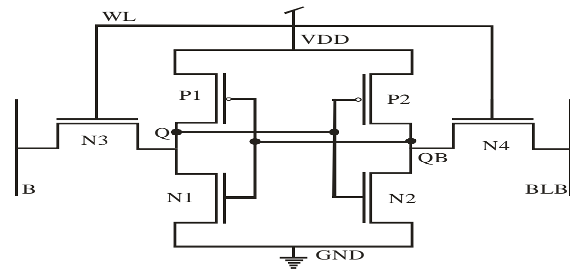

Figure 4: Schematic Diagram of 6T SRAM Cell

4. Proposed SRAM Using FinFET

To hold single bit data simply we are using SRAM and for large applications we can use array of SRAM. The noise immunity, leakage power, leakage current is the main issue in SRAM so to avoid this FinFET based SRAM is used [19]. FinFET based SRAM has same working as conventional based SRAM and the power dissipation, leakage is less in FinFET based SRAM. The SRAM and E-memory (Flash) MuGFET based help in cell issues, reduced leakage current and better device mismatch. The FinFET based design has low power working due to no body biasing and it works on less power supply but this power supply can be reduced up to certain value this value is data retention value [20]. The schematics are shown in Figure.3 and Figure.4.

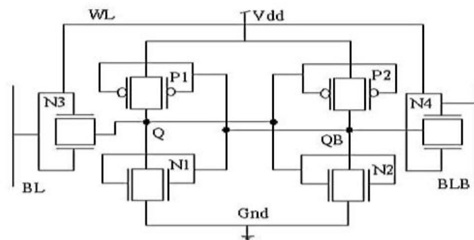

Figure 5: FinFET based 6T SRAM Cell

5. Effect of Leakage Current and Power

Power dissipation occurs due to charging and discharging of load capacitances, it refers to as the dynamic power dissipation. Dynamic power is consumed when switching in bits going on either "0" to "1" or "1" to "0". It provides the region of transistors works in active region and cutoff region, the current is:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{{V_{DS}}^2}{2} \right) \quad (6)$$

For active region, the current equation is:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} \right) \quad (7)$$

For saturation region, the current equation becomes:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left(\frac{{V_{DS}}^2}{2} \right) \quad (8)$$

Scaling down technology to a significant value increases the performance but total power consumption in some portion not decreases due to leakage parameters due to reduced threshold voltage and high packaging density [21]. ITRS in 2014 stated that 13% of feature size shrinks per year. The cost of memory also reduces because of bulk production of units. The gate oxide thickness reduces drastically as feature size reduces then gate tunneling leakage current increases [22].

Power dissipation has four components in digital circuits:

$$P = P_{ds} + P_{sc} + P_{sb} + P_{leakage} \quad (9)$$

In which P is the total power dissipation, P_{ds} is the dynamic-switching, P_{sc} is the short circuit, $P_{sb}$is the static-biasing and $P_{leakage}$is the leakage power.The power dissipation in dynamic-switching depends upon frequency, capacitor and supply voltage i.e.

$$P_{ds} = CV^2 f \quad (10)$$

The short circuit power dissipation is depends on τ rise time or fall time, and clock frequency *f.* The formula is:

$$P_{sc} = K(V_{dd} - 2V_{th})^3 \tau f \quad (11)$$

The flow of static current towards ground from supply voltage without input degradation is leakage power. Three leakage mechanisms are: Sub threshold, band to band tunneling (BTBT) and gate oxide.

$$I_s = I_o W e^{\frac{V_{gs} - (V_{t0} - \eta V_{ds} - \gamma V_{bs})}{n V_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}} \right] \quad (12)$$

Where I_s is sub threshold leakage current, $V_{t0}$the zero bias thresholds, n isthe sub-threshold slope coefficient, C_{ox} is the gate oxide capacitance.Band-to-Band-Tunneling is small and can be ignored andsub-threshold leakage current and gate tunneling leakage currents is taken into measure.

6. Delay

To determine delay of signal from input to output circuit during the high to low and vice versa at the output we use propagation delay times τ_{PHL} and τ_{PLH}.

We can define the τ_{PHL} is referred to the time delay which occurs with the 50% of the voltage transition of the rising input voltage and falling output voltage. Similarly, we can define the τ_{PLH} is referred to the time delay which occurs with the 50% of the voltage transition of the falling input voltage and rising output voltage. For simplification of the analysis and derive the delay expression, we have considered an input voltage waveform having zero rise and fall time acting as an ideal step pulse. Due to this assumption τ_{PHL} becomes the time consumed for the output voltage to fall from V_{OH} to 50% of the voltage level and τ_{PLH} becomes the time consumed for output voltage to rise from V_{OL} to 50% of the voltage level. The 50% of the voltage point is defined by

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OH} + V_{OL}) \quad (13)$$

Now we can define the average propagation delay τ_P of the inverter which gives the average time required for the input signal to propagate through the inverter[25]-[26].

$$\tau_P = \frac{\tau PHL + \tau PLH}{2} \quad (14)$$

Delay of the cell depends upon the time elapsed between the cell from input to output transition of the signal.

Table I: shows the comparison of different parameters of both conventional 6T and FinFET based 6T SRAM at 45nm technology in cadence virtuoso tool

Parameters	Conventional 6T SRAM		Finfet Based 6T SRAM	
	Write	**Read**	**Write**	**Read**
Technology	45 nm	45 nm	45nm	45nm
Supply	700 mV	700 mV	700mV	700mV
Leakage current	69.22 ×10^{-12} A	54.88×10^{-12} A	69.00×10^{-12} A	53.90 ×10^{-12} A
Leakage power	7.346 nW	1.710×10^{-6} W	7.561 nW	1.709 ×10^{-6} W
Delay	20.57 ns	21.70 ns	20.55 ns	21.44 ns

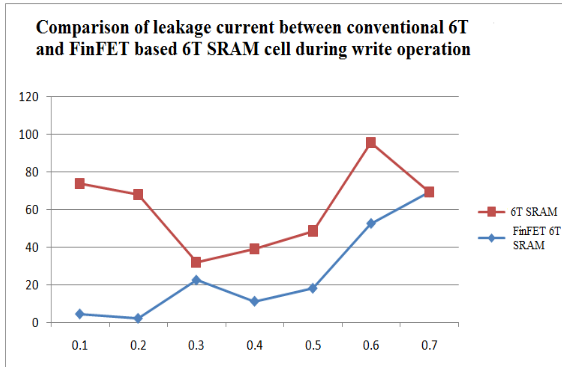

Figure 6: Comparison of leakage current between conventional 6T and FinFET based 6T SRAM cell during write operation

This figure illustrates the comparison of both conventional 6T and FinFET based 6T SRAM cell during write operation. From the figure, we can say that the leakage current of FinFET based 6T SRAM is less than 6T SRAM cell from 0.1V to 0.6V supply voltage but at 0.7V supply voltage the leakage current become equal at both conventional 6T and FinFET based 6T SRAM cell.

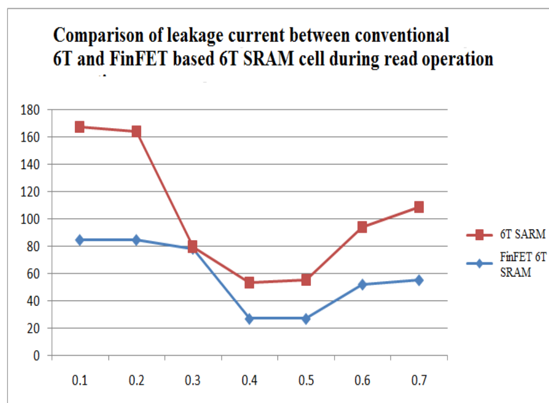

Figure 7: Comparison of leakage current between conventional 6T and FinFET based 6T SRAM cell during read operation

This figure illustrates the comparison of leakage current in both conventional 6T and FinFET based 6T SRAM cell through read operation. From the figure we can conclude that the leakage current of FinFET based 6T SRAM cell during read operation is less than the leakage current of conventional 6T SRAM cell.

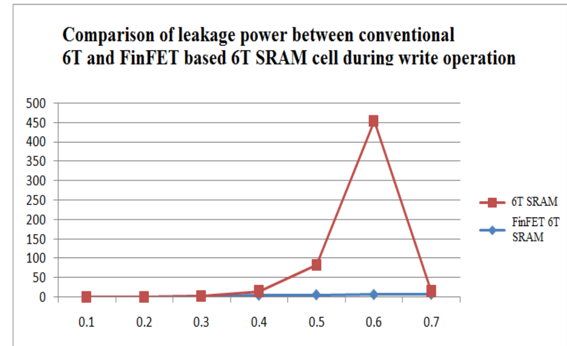

Figure 8: Comparison of leakage power between conventional 6T and FinFET based 6T SRAM cell during write operation

This figure illustrates the comparison of leakage power between conventional 6T and FinFET based 6T SRAM cell through the write operation. By seeing the figure we can conclude that for some supply voltages the leakage power of conventional 6T and FinFET based 6T SRAM cell is constant but after 0.4V supply voltage there is sudden rise in leakage power of conventional 6T SRAM cell and 0.7V supply voltage again the leakage voltage is become same.

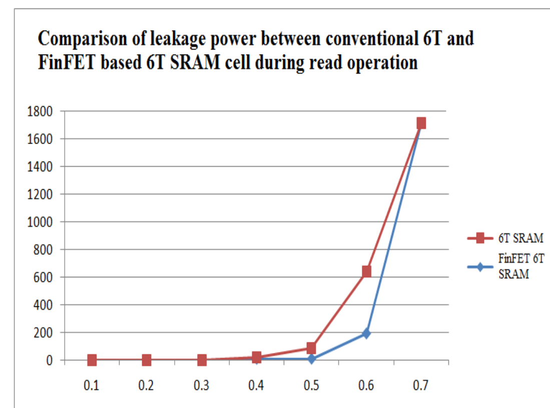

Figure 9: Comparison of leakage power between conventional 6T and FinFET based 6T SRAM cell during read operation

This figure illustrates the comparison of leakage power in both conventional 6T and FinFET based 6T SRAM cell during read operation. By seeing the we can say that at starting the leakage power of conventional 6T and FinFET based 6T SRAM cell is constant after then there is little increase in leakage

power of conventional 6T SRAM cell but at 0.7V of supply voltage it become constant.

7. Conclusion

For a high density and low leakage current, we propose a FinFET based 6T SRAM cell in which we perform both read and write operation and compare the result of both write and read operation with the conventional 6T SRAM cell operation. By comparing we can say that, FinFET based 6T SRAM cell possess low leakage current as compare to conventional 6T SRAM cell and delay is also reduced in both read and write operation, leakage power is also less in FinFET based 6T SRAM cell than 6T SRAM cell. These designs also improve the read and write stability. Also, we know that leakage current of any device doubles for every 10°Ctemperature. This simulation result is done at 45 nm technology with the help of cadence virtuoso tool.

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