Research Article

International Journal of Advanced Computer Research, Vol 8(39)
ISSN (Print): 2249-7277 ISSN (Online): 2277-7970
http://dx.doi.org/10.19101/IJACR.2018.838013

An efficient FPGA based NoC architecture for data communication

Vijayalaxmi Jamagoud[1*] and Satish S. Bhairannawar[2]
M.Tech in Digital Electronics, Department of Electronics and Communication Engineering, SDM College of Engineering and Technology, Dharwad, Karnataka, India[1]
Professor, Department of Electronics and Communication Engineering, SDM College of Engineering and Technology, Dharwad, Karnataka, India[2]

Received: 06-June-2018; Revised: 18-October-2018; Accepted: 30-October-2018

Abstract
In today's real time world network on chip (NoC) plays a major role in fast communication between entities. The need for NoC hardware is in demand based on requirement for fast communication with large data bandwidth. In this paper, an efficient field programmable gate array (FPGA) based NoC architecture for data communication is proposed. The router is designed with 4 ports using proposed controller unit, novel first-in first-out (FIFO) architecture and XY routing logic. The proposed controller unit comprises of MUX based architecture to support the data transfer in East, West, North and South directions using respective select lines with flip-flops connected to the output of multiplexers to achieve delay synchronization. A novel FIFO architecture is designed using a counter and decision unit which are used to keep track of incoming data using signal mem_empty or mem_full. The XY routing logic is used to communicate between the routers and a test sample data is chosen to validate the routing path between source and destination using XY routing logic. The proposed routing architecture is tested on SPARTAN-6-XC6SLX45 board. It is observed that the performance parameters such as slice registers, power dissipation and maximum operating frequency are 290, 38.35 mW and 220.729 MHz respectively.

Keywords
NoC, Controller unit, FIFO, XY routing algorithm.

1.Introduction
NoC is a new model in which a single silicon chip is utilized to execute various communication features used in substantial to huge scale integration systems. NoC is another change to the universe of systems and also the other way to deal with disadvantages like wiring delay. There are numerous types of interconnections like point-to-point, bus architecture, carbon nanotubes, optical fiber [1] where NoC perform is better to reduce the interconnection issues in future designs. System on chips designed using NoCs are getting popular in these days which provide solutions to the problem related to bus based designs and considered as the future of the application specific integrated circuit (ASIC) design [2]. NoC basically has three building blocks router, links and network adapter (NA) [3]. NoC approach has numerous benefits over traditional bus method and also provides high throughput as buses are less scalable and limited bandwidth [4].

The popularity of reconfigurable systems, paved the way for incorporating NoC protocol architectures on these boards. There exist many challenges to implement NoC protocoler according to the specifications of reconfigurable boards with proper optimization techniques. The focus of this work is to meet requirements like less area, power and high performance.

In existing architectures [5] buffers were replaced by virtual channel router architecture with adaptive inter port buffer sharing [6] which consumed less area and power. NoC routers consume more leakage power even when routers are not in use and this issue is solved by fine grained power gating to unused routers. The buffer redundancy issue is solved by buffer shared router architecture and defect tolerant algorithm which increases the reliability of NoC and also it can reduce the power consumption as discussed in literature [7]. The core router architecture [8] is proposed with low power idle (LPI) to analyse energy saving effect on optical burst switching (OBS) networks which decreases consumption of energy at low offered load. A new

*Author for correspondence

pipelined router [9] is designed and focused only on router latency reduction, which decreases the latency and increases the router area. The increase in IP core further increases the complexity of clock distribution in NoCs. In [10, 11], globally locally synchronous (GALS) architecture is proposed by making a connection from asynchronous clock to synchronous blocks and latency is improved. Further Elastic buffer architecture is introduced to support for virtual channels and to minimize the need of the buffers which facilitates both single cycle and two stage pipeline operation. The different types of routing [12] with guaranteed service (GS) arbitration are easily plugged into the router, which indicates that there is improvement in jitter. A reliable NoC router architecture [13] is proposed which has the ability to tolerate both hard and soft errors in the pipeline routing using existing techniques with spatial redundancy, exploitation of idle cycles, bypassing of faulty resources and selective hardening.

The fault tolerant router architecture is proposed in [14] which can avoid processing element (PE) isolation even if the router fails. The use of decimal matrix code (DMC) router [15] is designed, can correct and detect five bits at a time and loop back module is used to reroute the packets when a neighbouring node disappears instantaneously. The 4x4 mesh topology is implemented by making use of virtual channels (VCs) approach in [16]; it can minimize the path assign processing time and increase the performance speed of the NoC architecture. The power efficient, scalable router architecture is designed and implemented [17] on FPGA board by using virtualized merged (VM) approach. In this approach three optimizations are integrated into the basic VM approach to decrease the dynamic power dissipation. The 8 ports NoC architecture designed [18] which plays an important role in providing timing attributes and decreases the latency in the network. Previous routers have lower performance speed due to its complexity with higher number of slice LUTs [19−23] and consume more power [24]. Therefore, this study proposed a new NoC router architecture using a novel FIFO architecture with the XY routing algorithm for an efficient FPGA based NoC router architecture with high speed and low power consumption.

2.Materials and methods

2.1Proposed router

The proposed NoC router architecture is targeted for high speed and low power requirements. It comprises of a proposed controller unit, novel FIFO unit synchronized with routing logic consisting of 4 ports, namely East, West, North and South is as shown in *Figure 1*. The router operation is initiated with a data transfer request between source and destination router. The routing logic decides the direction of data transfer based on availability of FIFO and the controller unit synchronized all the blocks till data is transferred from source and destination. The proposed router can also be called as Quad Core system having four inputs, data_in_w, data_in_e, data_in_s and data_in_n and similarly four outputs, data_out_w, data_out_e, data_out_s and data_out_n respectively. It consists of controller unit, which controls the operation of all the ports and four FIFOs, one FIFO for each port and designed with buffer depth of 3 and buffer width of 13 bits. The controller unit selects the direction of data transmission based on data availability check on respective FIFOs. These FIFOs have to be synchronized with routing logic for proper routing of data's between source and destination. All the FIFOs are identical to each other and synchronized with XY routing block.

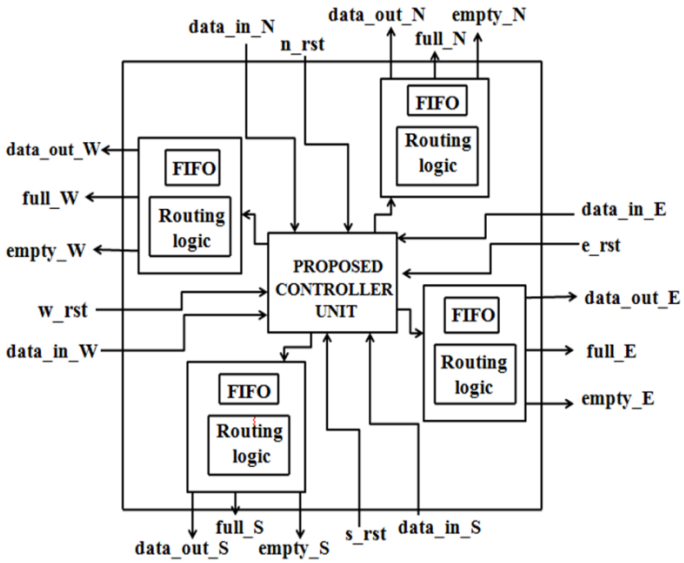

Figure 1 Proposed router architecture

2.2XY routing algorithm for 2×2 network

The most popular XY routing algorithm [19] is proposed by Wang Zhang and Ligang Hou in 2009. Based on literature [21], this study considered XY routing algorithm with 2×2 Mesh topology consisting of 4 nodes to validate data transfer as shown in *Figure 2*. The source and destination router node have to be identified before the transfer of data. Each router having co-ordinates as (x, y) for the routing current address (Cx, Cy) is compared with the destination router address (Dx, Dy). The data is

transferred from the current router to the next router either in X direction or in Y direction based on the comparison with output addresses of the source and destination. This process repeats until the data reaches the destination address. The pseudo code for XY routing is shown in *Table 1*. The destination node address in the X direction is compared with the current source node address. If the destination address is greater than the source, then the data is transferred in south direction through south port else the data is transferred in north direction through north port. Similarly, if the destination node address in Y direction is greater than the current source node address then the data is transferred in east direction through east port else the data is transferred in west direction through west port.

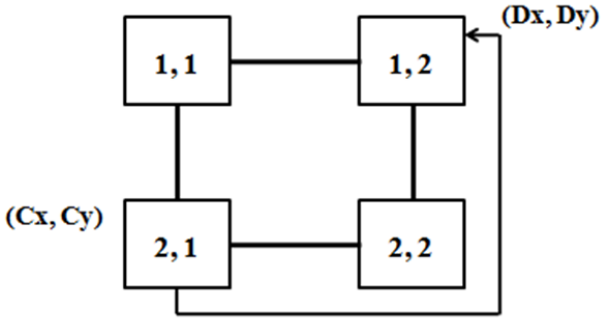

Figure 2 2×2 mesh topology

Table 1 Pseudo code for XY routing

- Choose source node
- Choose destination node
- *If (dx>cx)*
  south_port<=data_in;
  else if (dx<cx)
  north_port<=data_in;
  else if (dy>cy)
  east_port<=data_in;
  else
  west_port<=data_in;
  end if;
- Next repeat for any other path

2.3Proposed FIFO architecture

Each router consists of buffer through which the data is transmitted every time as shown in *Figure 3*. In this design, each port is designed with buffer depth of 3 using D-flip-flops and buffer width of 13 bits. The depth of FIFO is arrived with many trails to improve the performance of the system. The clock, reset and request inputs are used for D-flip-flop in synchronous to achieve high data transmission. The counter, which counts the data every time with decision block will keep track of memory usage. If there is no enough memory to store the data, then it indicates the status as mem_full output. If the port is idle, then it activates the status as empty through port mem_empty which indicates it is ready to receive data. This operation remains same for all the ports with proper synchronization.

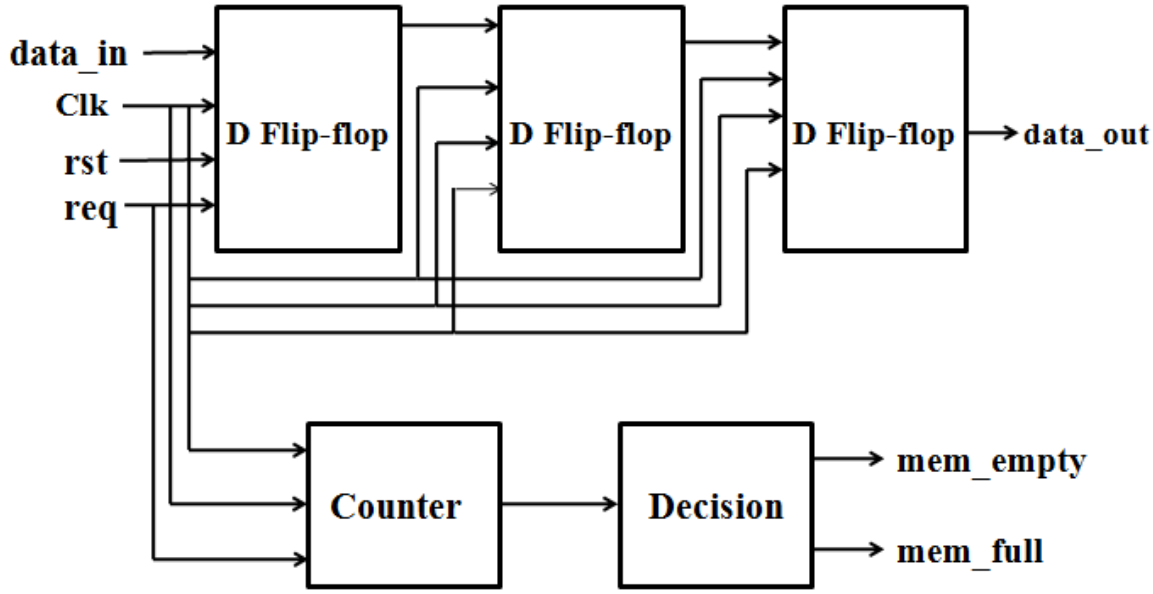

Figure 3 Proposed FIFO architecture

2.4Proposed controller unit

The proposed control unit is designed by using multiplexers, D-flip-flops and De-multiplexer as shown in *Figure 4*. The controller unit plays major role in data transfer. The multiplexers are connected in parallel to receive the data inputs from 4 different ports and are synchronized by port_sel line. The controller unit is used to select the respective output and the input line, according to the select line. The port_sel line which is used to select the input port and the n_rst, e_rst, w_rst and s_rst lines are used to select the output ports through de-multiplexer. Multiplexers are used to route the incoming data and similarly de-multiplexer is used to route outgoing data. It can route only a single channel input at a time and four D-flip-flops are used at the output side of multiplexers for the delay synchronization purpose. The data_in_e, data_in_w, data_in_s and data_in_n are the inputs to the multiplexer. The port_sel of the multiplexer is of data width 2 bits which activates any one multiplexer based on data availability on FIFO which is further decided by the XY routing algorithm. The concept of the proposed controller unit is taken from [20].

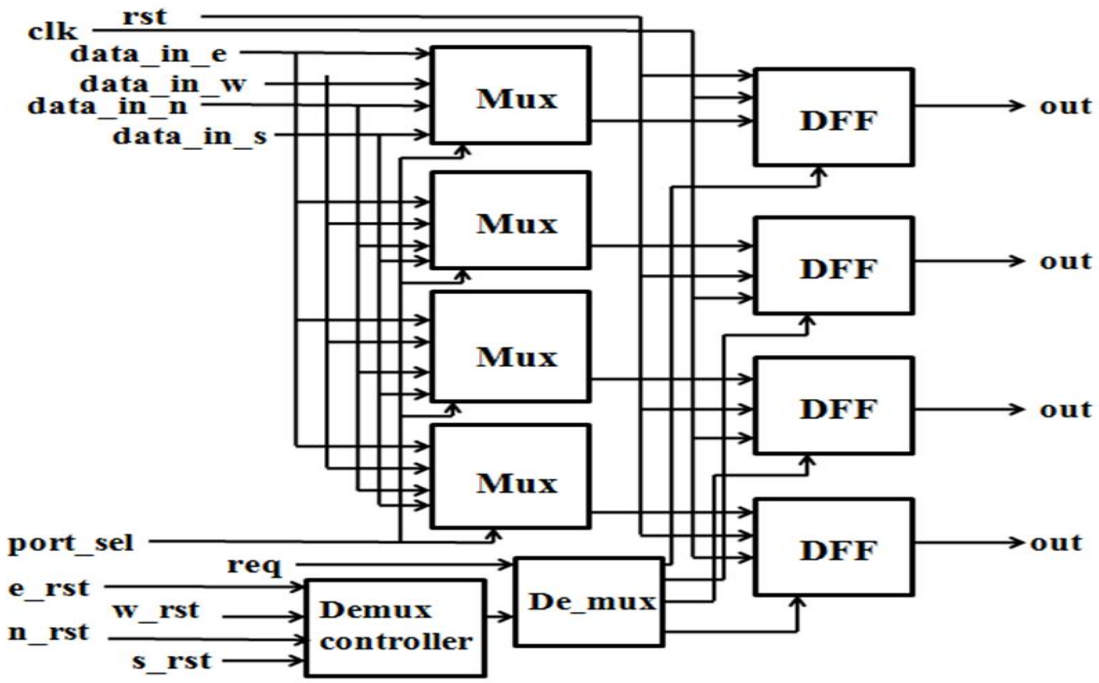

Figure 4 Proposed controller unit

2.5Performance validation

The proposed router is tested for the performance using different trails of data transfer between source and destination routers. The entire architecture is synthesized to validate the maximum operation speed of 220.729MHz with power of 38.35mW.

3.Result and discussions

The proposed router is simulated and synthesized using Xilinx ISE 14.5 on SPARTAN-6 XC6SLX45-3FGG484 FPGA.

3.1Simulation result of proposed router

The simulation result of proposed router with 2 bit port select line which selects the output port and sends the data to selected output port is shown in *Figure 5*. For example, when a port select line is 01 it means it is west port with De-MUX line is 11 which indicates the south port, then data_in-w[12:0] that is "1111111111100" is sent from west to south output port (c_s[12:0]) as shown in *Figure 6*.

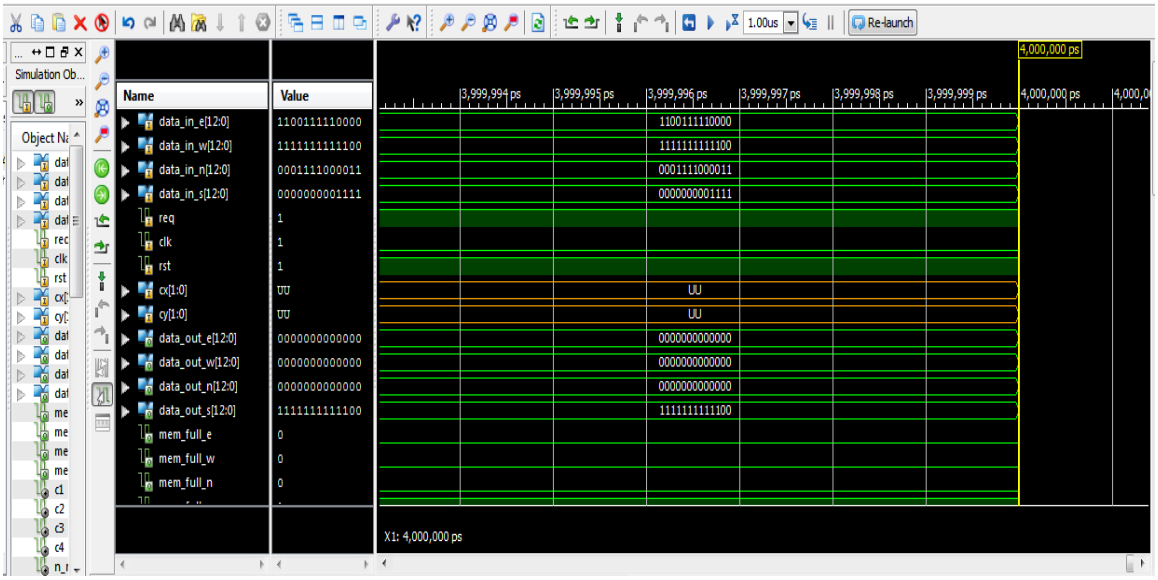

Figure 5 Simulation result of proposed router with inputs and outputs

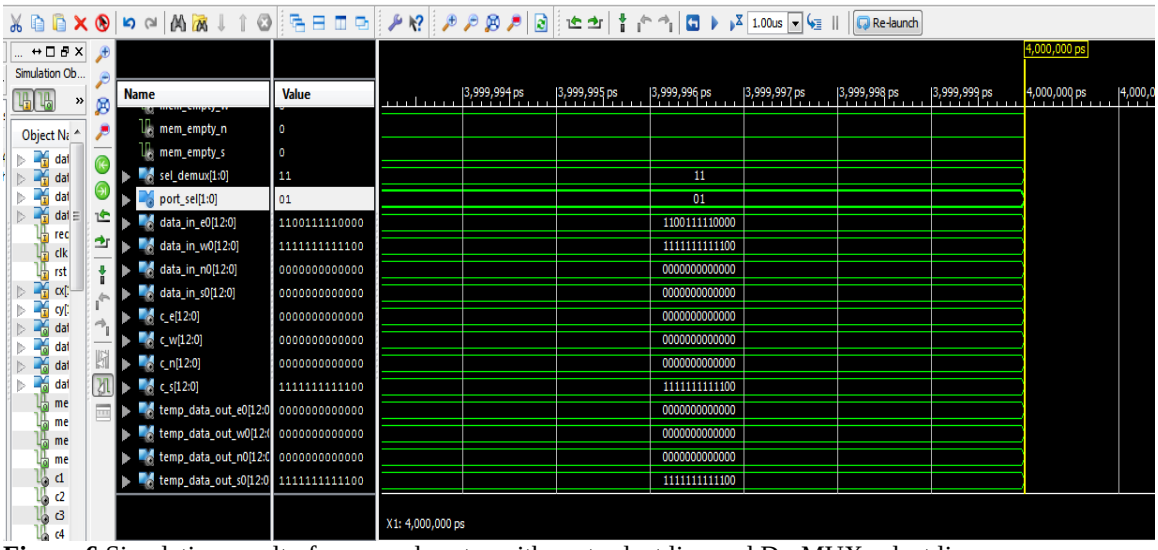

Figure 6 Simulation result of proposed router with port select line and De-MUX select line

3.2Proposed router synthesis results

The hardware resource utilization of proposed router is shown in *Table 2*. It consumes 290 slice registers with a maximum operating speed of 220.729 MHz. It also uses 149 fully used LUT-FF pairs with static power of 36.07 mW and dynamic power of 2.28 mW resulting in a total power of 38.39 mW. These results are better compared to existing architectures since we use a dynamic FIFO technique.

3.3Comparison of existing routers with proposed router

The comparison of performance parameters with respect to hardware resources to validate our proposed router. From *Table 3*, NoC with Predominant routing algorithm and dual crossbar arrangement increases the number of slice registers. Unified buffer in bidirectional NoC router gives more operating frequency compared with proposed router. Reconfigurable NoC router designed with power gating technique increases the number of slice LUTs. NoC architecture with smart power saving (SPS) algorithm increases the number of slice registers. Meanwhile, the proposed method have the lowest number slice register which decreases the complexity in terms of slice LUTs and increases the operating speed and reduces the power consumption.

Table 2 Synthesis results of proposed router

Sl. No	Parameter	Results
1.	Number of slice registers	290
2.	Number of slice LUTs	217
3.	Number of fully used LUT-FF Pairs	149
4.	Maximum operating frequency (MHz)	220.729
5.	Static power (mW)	36.07
6.	Dynamic power (mW)	2.28
7.	Total power (mW)	38.35
8.	Delay (ns)	4.530
9.	Bounded IOBs	115

Table 3 Performance based on hardware resources

Router architecture	NoC with predominant routing algorithm and dual crossbar [21]	Bidirectional NoC with buffer [22]	Reconfigurable NoC with power gating technique [23]	NoC architecture with SPS algorithm and clock control circuit [24]	NoC with novel FIFO architecture and XY routing algorithm (proposed router)
Board	Virtex-5 XC5VLX50	Virtex-2 XC2VP30	Spartan -6	XC5VLX50T-LFFLI36	Spartan-6 XC6SLX45
Number of slice registers	1322	529	----	785	290
Number of slice LUTs	1022	954	235	-----	217
Number of fully used LUT-FF pairs	----	523	-----	-----	149
Maximum operating frequency (MHz)	----	226.19	-----	-----	220.729
Power(mW)	-----	-------	-----	257.05	38.35
Number of ports	2×2 Network	5	4	-----	4

4.Conclusion

The main idea of our work is to design an efficient NoC router architecture to meet requirements such as power dissipation, less number of slice LUTs and slice registers. In this paper, an efficient FPGA based NoC architecture for data communication is proposed. The router is designed with 4 ports using proposed controller unit, novel FIFO architecture and XY routing logic. The simulation of the proposed architecture is performed by using Xilinx ISE 14.5 Isim tool and tested on SPARTAN XC6SLX45 FPGA board. The comparison of the proposed architecture with existing architectures is done and it is observed that the performance parameters such as slice LUTs, slice registers, power dissipation and maximum operating frequency are better than existing Router architectures.

Acknowledgment

None.

Conflicts of interest

The authors have no conflicts of interest to declare.

References

[1] Bhanwala A, Kumar M, Kumar Y. FPGA based design of low power reconfigurable router for network on chip (NoC). In international conference on computing, communication & automation 2015 (pp. 1320-6). IEEE.

[2] Kumar M, Kumar K, Gupta SK, Kumar Y. FPGA based design of area efficient router architecture for network on chip (NoC). In international conference on computing, communication and automation 2016 (pp. 1600-5). IEEE.

[3] Shermi S, Arun CS. A novel architecture of bidirectional NoC router using flexible buffer. In international conference on emerging technological trends 2016 (pp. 1-6). IEEE.

[4] Sharma N, Gadag S. An efficient way to increase performance by using low power reconfigurable routers. IOSR Journal of Electronics and Communication Engineering. 2013; 8(6):39-44.

[5] Langar M, Bourguiba R, Mouine J. Virtual channel router architecture for network on chip with adaptive

inter-port buffers sharing. In international multi-conference systems, signals & devices 2016 (pp. 691-4). IEEE.
[6] Mondal HK, Gade SH, Kishore R, Deb S. Power and performance-aware fine-grained reconfigurable router architecture for NoC. In sixth international green and sustainable computing conference (IGSC) 2015 (pp. 1-6). IEEE.
[7] Xia L, Ma Y, Xu N. Defect-tolerant routing algorithm for low power NoCs based on buffer-shared router architecture. In international conference on communications, circuits and systems 2013(pp. 391-4). IEEE.
[8] Yang W, Jung JH, Kim YC. Performance evaluation of energy saving in core router architecture with low power idle for OBS networks. International conference on information networking 2012 (pp. 318-23). IEEE.
[9] Roca A, Flich J, SIlla F, Duato J. A latency-efficient router architecture for CMP systems. In euromicro conference on digital system design: architectures, methods and tools 2010 (pp. 165-72). IEEE.
[10] Cheshmi K, Trajkovic J, Soltaniyeh M, Mohammadi S. Quota setting router architecture for quality of service in GALS NoC. In international symposium on rapid system prototyping 2013 (pp. 44-50). IEEE.
[11] Seitanidis I, Psarras A, Dimitrakopoulos G, Nicopoulos C. Elastistore: an elastic buffer architecture for network-on-chip routers. In proceedings of the conference on design, automation & test in Europe 2014 (pp.1-6). European Design and Automation Association.
[12] Ramani S, Sundararajan J. A case study on NoC router architecture for optimizing the latency. In international conference on advanced computing and communication systems 2013 (pp. 1-4). IEEE.
[13] Poluri P, Louri A. Shield: a reliable network-on-chip router architecture for chip multiprocessors. IEEE Transactions on Parallel and Distributed Systems. 2016; 27(10):3058-70.
[14] Yan P, Jiang S, Sridhar R. A novel fault-tolerant router architecture for network-on-chip reconfiguration. In international system-on-chip conference 2015 (pp. 292-7). IEEE.
[15] Jayan G, Pavitha PP. FPGA implementation of an efficient router architecture based on DMC. In international conference on emerging technological trends 2016 (pp. 1-6). IEEE.
[16] Shenbagavalli S, Karthikeyan S. An efficient low power NoC router architecture design. In online international conference on green engineering and technologies 2015 (pp. 1-8). IEEE.
[17] Haria S, Ganegedara T, Prasanna V. Power-efficient and scalable virtual router architecture on FPGA. In international conference on reconfigurable computing and FPGAs 2012 (pp. 1-7). IEEE.
[18] Fatima A, Waseem SM. Rapid on-chip communication in 2D networks using 8-port router in a multicast environment and their realization. International Journal of Science and Research. 2014; 3(9):117-20.
[19] Chawade SD, Gaikwad MA, Patrikar RM. Review of XY routing algorithm for network-on-chip architecture. International Journal of Internet Computing. 2012; 1(4):48-52.
[20] Sahu S, Kittur HM. Area and power efficient network on chip router architecture. In conference on information & communication technologies 2013 (pp. 855-9). IEEE.
[21] Suraj MS, Muralidharan D, Kumar KS. A HDL based reduced area NOC router architecture. In international conference on emerging trends in VLSI, embedded system, NANO electronics and telecommunication system 2013 (pp. 1-3). IEEE.
[22] Khodwe A, Bhoyar C N. Area efficient FPGA based bidirectional network on chip router through virtual channel regulator. International Journal of Computer Trends and Technology.2013; 4(7):2107-12.
[23] Yadav MP, Singh MA. Area efficient router architecture design of network-on-chip (NOC). International Research Journal of Engineering and Technology.2016; 3(6):555-8.
[24] Basha SS, Babu TR. Design of intelligent power saving (IPS) architecture for reducing power and area in NoC. In international conference on innovations in information, embedded and communication systems 2015(pp.1-8). IEEE.

Vijayalaxmi Jamagoud was born in Karnataka, India in 1994. She received the BE degree in Electronics and Communication from S. G. Balekundri Institute of Technology, Belagavi, Karnataka, India in 2016. She pursued her M. Tech in Digital Electronics from SDM College of Engineering and Technology, Dharwad, Karnataka, India in 2018.
Email: vijujamagoud@gmail.com

Satish S Bhairannawar was born in Karnataka, India, in 1979. He received the B.E. degree in Electronics & Communication from Sir M. Visvesvaraya Institute of Technology, Bangalore University, Bangalore, India, in 2001. He obtained his M.E in Electronics and Communication Engineering in 2005 from University Visvesvaraya College of Engineering, Bangalore. He was awarded Ph.D for "Efficient VLSI Architectures for Fingerprint Recognition" in 2015, from University Visvesvaraya College of Engineering, Bangalore University.
Email: satishbhairannawar@gmail.com