Research Article

International Journal of Advanced Computer Research, Vol 8(38)
ISSN (Print): 2249-7277 ISSN (Online): 2277-7970
http://dx.doi.org/10.19101/IJACR.2018.838014

Design and implementation of Haar wavelet packet modulation based differential chaos shift keying communication system using FPGA

Rawaa Abed Mohammed[1*], Fadhil Sahib Hassan[2] and Mohammed Joudah Zaiter[3]
Research Scholar, Department of Computer Engineering Technology, Electrical Engineering Technical College, Middle Technical University, Baghdad, Iraq[1]
Assistant Professor, Department of Electronics and Communication Engineering, Mustansiriyah University, Iraq[2]
Lecturer, Department of Computer Engineering Technology, Electrical Engineering Technical College, Middle Technical University, Baghdad, Iraq[3]

Received: 19-July-2018; Revised: 18-September-2018; Accepted: 21-September-2018

Abstract
Efficient design and implementation of Haar wavelet packet modulation based differential chaos shift keying (HWPM - DCSK) using field programmable gate array (FPGA) platform was proposed. A fast algorithm for Haar wavelet packet transform (FHWPT) was used to enhance the complexity of the wavelet packet modulation (WPM) system. The HWPM-DCSK system uses sixteen points of FHWPT and inverse fast Haar wavelet packet transform (IFHWPT) with spreading factor about eight for DCSK modulation. The suggested system was designed using a Xilinx system generator (XSG) tool. Software tools used in this work include ISE 14.5. A Virtex-4 (xc4vfx100-12ff1152) board was used for the implementation. The results are showing that the information bits are recovered successfully at the receiver side. The system was routed successfully with the resources of 5% slice flip flop, 5% look-up table (LUT), 10% occupied slices and 70% digital signal processing (DSP) 48s numbers from the selected device. The XSG is more reliable, flexible, easier, and gives the optimum design for the FPGA technicality via comparing with the conventional FPGA design. Also, the hardware simulation results show that the proposed system is efficient in performance for the real time communication system with low consuming power.

Keywords
Wavelet packet modulation, Haar wavelet filter, Fast wavelet transform, Differential chaos shift keying, Non-coherent spread spectrum communication system, XSG, FPGA.

1.Introduction
The chaotic signals are described as random-like; change its behavior with the initial condition. It's non-periodic and due to wide band property the signal is suitable for the spread spectrum modulation. A number of chaos based modulation has been mentioned [1]. Without the need for channel estimation and chaotic synchronization, non-coherent chaos-based schemes have attached to a lot of attention. The differential chaos shift keying (DCSK) system is considered as a kind of non-coherent systems [2]. In DCSK system, the information and the reference bearing signals are separated by time slots and translated in the same channel. The main drawback of DCSK systems is the receiver requires a radio frequency (RF) delay line, which is not simple to integrate in complementary metal-oxide-semiconductor (CMOS) technology. Sending non-information bearing reference samples spent half of bit duration, which leads to low data rate and energy efficiency [2].

In recent years, the multicarrier techniques are combined with DCSK to improve the data rate, energy efficiency and RF delay line [3−10]. In [3] and [4] the authors propose a multicarrier modulation with DCSK (MC-DCSK). In [5] orthogonal frequency division multiplexing (OFDM) is combined with DCSK system and named OFDM-DCSK. While in [6] Hasan combines OFDM and short reference quadrature chaos shift keying (OFDM-SRQCSK) and study the analysis of the system under additive white Gaussian noise (AWGN) and multipath Rayleigh fading channels. Further studies include a hybrid multicarrier DCSK and multi-users, like a multiuser MC-DCSK (MU MC-DCSK) [7], Analog network coding for MU MC-DCSK [8] and multiuser OFDM-based DCSK (MU

*Author for correspondence

OFDM-DCSK) [9]. In addition, a multicarrier with chaos shift keying (MC-CSK) is presented in [10]. In recent years another type of multicarrier modulation (MCM) is emerged named wavelet packet modulation (WPM) [11]. WPM has been improved compared to OFDM. The major core of WPM is the wavelet packet transform (WPT) which needs real arithmetic operation while the major core of OFDM is the fast Fourier transform (FFT) which needs a complex operation [11, 12]. WPM is shared all the advantages of multicarrier technique and offered more advantages like higher efficiency because removal of Guard Interval (GI). It has been considered such as one of wavelet transforms which have been well localized both in time and frequency domain, whereas sinusoid waveforms have been only localized in the frequency domain. WPM has been additional fascinating merits patrimonial from the wavelet packet [11] . Efficient realizations are needed to implement DCSK and WPM systems. In communication systems, the digital implementation is more immune to the imperfections of real electronic systems and due to the easiness of encryption it's more secure and shows greater noise immunity. Furthermore, they have consisted of components to digital circuit which are inexpensive and produced easily onto a single chip [13]. Field programmable gate array (FPGA) technique is the most flexible and efficient design with high clock rates that can be used to realize digital communication systems. In [14] efficient FPGA design of DCSK system is proposed using the DSP builder technique. The authors in [15] and [16] proposed a fast algorithm to implement Haar WPM system and then realized using FPGA technique. In this paper, we combine Haar WPM and DCSK (HWPM-DCSK) system in a sufficient way to improve the performance of DCSK. The HWPM-DCSK proposed system is implemented using a Xilinx system generator (XSG) in FPGA. XSG is a plug-in to Simulink that can design to improve high-performance digital signal processing (DSP) systems for Xilinx FPGAs. The synthesizable hardware description language (HDL) code can be mapped to Xilinx pre-optimized algorithms will be created by using this tool. This hardware description language design can be then synthesized to implement on Xilinx FPGAs [17, 18]. In this paper, a new multicarrier based DCSK is called WPM-DCSK system is introduced. This proposed system is a development of the OFDM-DCSK system. All the analysis and comparison of WPM-DCSK with OFDM-DCSK are introduced in the previous paper. Therefore, only the hardware implementation of the proposed system in the FPGA is presented in this paper. The proposed system is implemented using XSG packages that offer a number of advantages over the existing implementation platforms.

2.Fast Haar wavelet packet transform

The inverse fast Haar wavelet packet transform (IFHWPT) and fast Haar wavelet packet transform (FHWPT) are derived in detail in [14, 15]. The signal flow graphs of IFHWPT and FHWPT for 8-points are shown in *Figure 1*. To reconstruct the exact received signal from the flow graph in *Figure 1*, the FHWPT output is normalized by the factor 2^k, where k is staged level. This normalization can be achieved by shifting the results k times. The parallel symbols x_i ,i=1,..,8 are the input symbols of IFHWPT and $\tilde{x}_i$, i=1,.., 8 are the output symbols of FHWPT. For higher numbers of subcarriers, the flow graph of FHWPT and IFHWPT can be deduced in the same manner. It can be seen that this algorithm don't need for multiplication and division only need is addition, subtraction and simple shifting operation. FHWPT or IFHWPT requires $k2^k$ addition numbers [14, 15]. For example in 8-points FHWPT there are 3 stages level and 24 addition numbers.

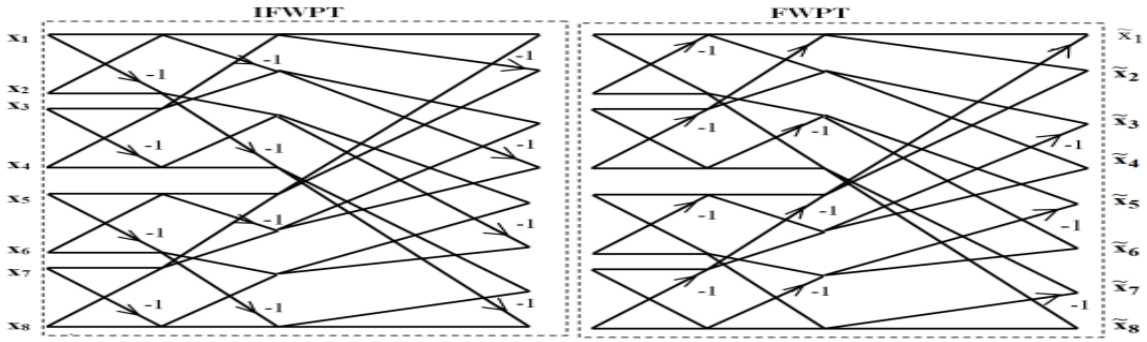

Figure 1 The signal flow graphs of IFHWPT and FHWPT

3.HWPM-DCSK communication system

Figure 2 illustrates the architecture of the HWPM-DCSK transmitter side. In the first, each stream bits b_j is mapped into d_u symbol where $d_u \in \{1,-1\}$ using binary phase shift keying (BPSK) modulation. Then, the u^{th} symbols are converted into parallel symbols $d_{u,p}$ (p=1,…., M) using serial to parallel converter. The same chaotic reference signal for each u^{th} frame has been multiplied by every p^{th} symbol in order to obtain the p^{th} information chaotic sequence, $d_{u,p}\ x_{u,k}$ for the u^{th} frame. In every M symbols, the single chaotic reference sequence is used in order to get better spectral efficiency and energy for every bit. For β spreading factors there are β of IFHWPT modulation obtained to get one symbol of HWPM-DCSK system. The total frame length of HWPM-DCSK is β (1+M) samples.

In this system, the second order Chebyshev polynomial function (CPF) is used to generate the chaotic signal [2].

$$x_{k+1} = 1 - 2x_k^2 \qquad (1)$$

The complete transmitted sequence of HWPM-DCSK symbols at the u^{th} time will be expressed in the following matrix $O_u \in \mathbb{R}_{(M+1)\times\beta}$ as:

$$G_u = \begin{bmatrix} x_{u,0} & x_{u,1} & x_{u,\beta} \\ d_1^u x_{u,0} & d_1^u x_{u,1} & d_1^u x_{u,\beta} \\ d_2^u x_{u,0} & d_2^u x_{u,1} & d_2^u x_{u,\beta} \\ \vdots & \vdots & \vdots \\ d_p^u x_{u,0} & d_p^u x_{u,1} & d_p^u x_{u,\beta} \\ \vdots & \vdots & \vdots \\ d_P^u x_{u,0} & d_P^u x_{u,1} & d_P^u x_{u,\beta} \end{bmatrix} \qquad (2)$$

The IFHWPT process has been applied to every k^{th} column vector of G_u matrix to obtain the transmitted signal of the HWPM-DCSK system. The number of the subcarriers of FHWPT is NFHWPT=M+1. The u^{th} IFHWPT transmitted signal of the k^{th} column is constructed as the sum of $\varphi_n(v)$ waveform individually modulated by the DCSK signal as follows.

$$s_u(k,v) = \sum_{n=0}^{N_{FWPT}-1} G_u(n,k)\ \varphi_n(v - N_{FWPT}) \quad , \quad \begin{matrix} v = 0,\dots,N_{FWPT}-1 \\ k = 0,\dots,\beta-1 \end{matrix} \qquad (3)$$

Where the $G_u(n,k)$ is the u^{th} frame of DCSK signal of k^{th} spreading and n^{th} samples, $\varphi_n(v)$ is the Haar wavelet filter reconstruction on the n^{th} subband of v^{th} synthesis bank.

Figure 2 illustrates the receiving side of HWPM-DCSK system. Firstly, FHWPT have been taken through all the number of the subcarrier N_{FHWPT} to the u^{th} received signalR_u. The u^{th} demodulated signal of FHWPT at the k^{th} spreading and n^{th} sub-band has been written like as [15].

$$r_t(k,n) = \sum_{v=0}^{N_{FWPT}-1} R_u(v,k)\ \psi_n(kN_{FWPT} - v) \quad , \quad \begin{matrix} n = 0,\dots,N_{FWPT}-1 \\ k = 0,\dots,\beta-1 \end{matrix} \qquad (4)$$

The $\psi_n(v)$ refers to the Haar wavelet filter decomposition of the n^{th} subband of v^{th} decomposition bank. The u^{th} received signal $r_u(k,n)$ is rewritten as $r_{u,(k+m\beta)}$, m=0,1,.., M and k=0,…, $\beta-1$, where for m=0 the signal represents the chaotic reference sequence while for m=1 the signal represents the first bit chaotic information sequence at the receiver side and so on. To detect the m^{th} bit, m=1,..,M, the correlation process is performed between the m^{th} bit and reference sequences are taken according to:

$$L_m^u = T_l \sum_{k=0}^{\beta-1} r_{t,k} r_{t,k+m\beta} \quad , m = 1,\dots,M \qquad (5)$$

Then, the demapping process has been performed on the output of the m^{th} correlator to get the m^{th} transmitted bit. At the end, the parallel M bits have been converted to the serial bits using parallel to serial converter. *Figure 3* shows the HWPM-DCSK receiver.

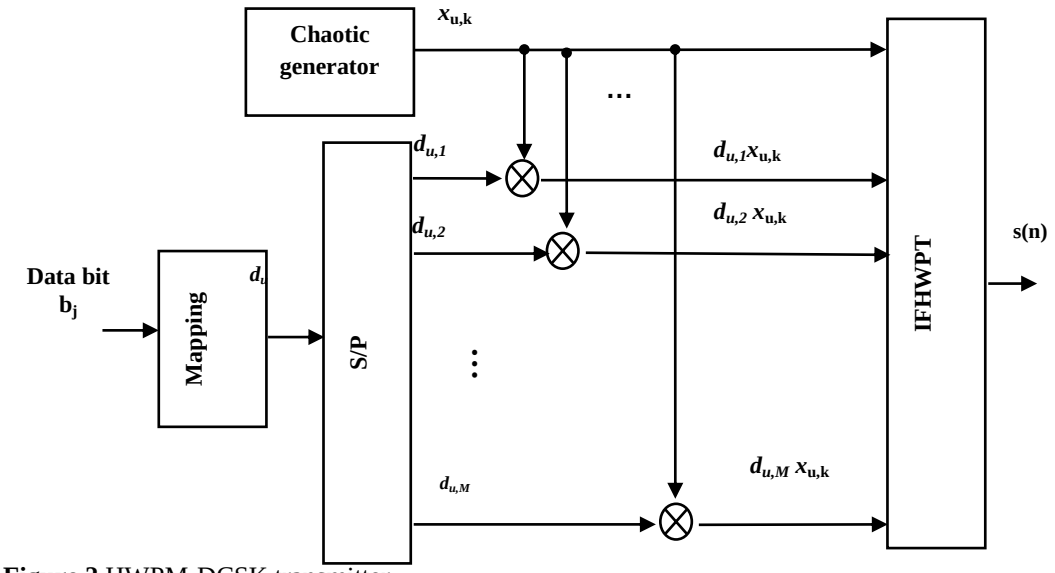

Figure 2 HWPM-DCSK transmitter

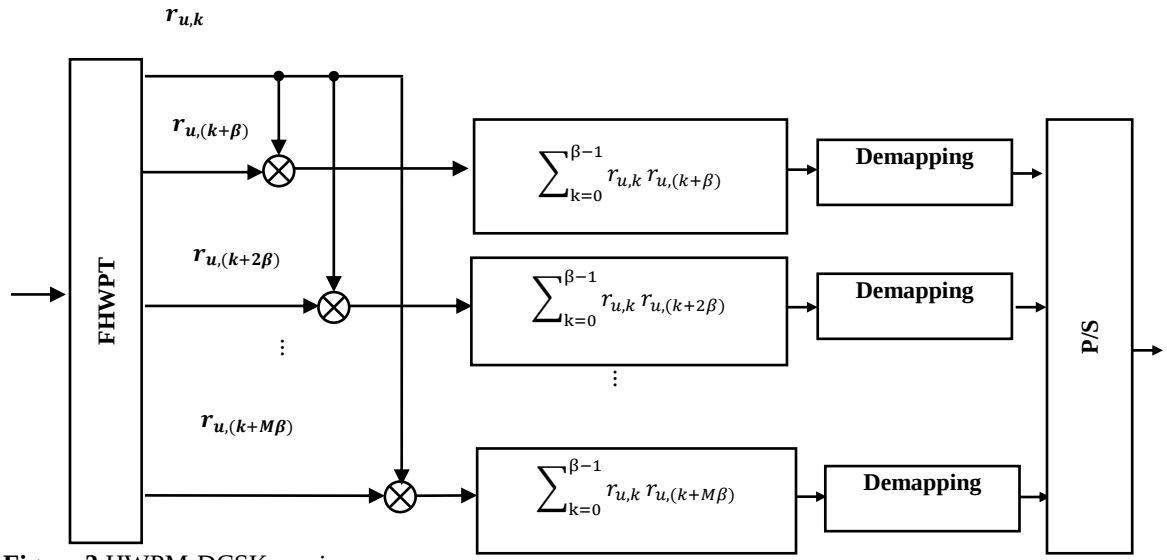

Figure 3 HWPM-DCSK receiver

4.HWPM-DCSK implementation using a Xilinx system generator

Figure 4 shows the block diagram of the HWPM-DCSK transceiver system. Every block in the system is designed using XSG where the period of the master clock is 10 ns. At the transmitter side, the Bernoulli binary signal generator can be used to generate the random bit generator with a rate 100 Mbps. The serial bits are converted into 8 parallel bits using serial to parallel converter. The rate is changed to 12.5 Mbps.

Each bit in the parallel sets is mapped into either +1 or -1 using the mapping function depends whether is 1 or 0 values respectively. Then, the symbol is spread using DCSK system. After that, the DCSK sequence is passed through the IFHWPT to produce the multicarrier signal, and then the signal is corrupted by AWGN channel. On the receiver side, the reverse operations of transmitters have been performed to recover the bits binary stream. The next subsections include the descriptions in detail for each block.

Table 1 shows the implementation parameters of the proposed system.

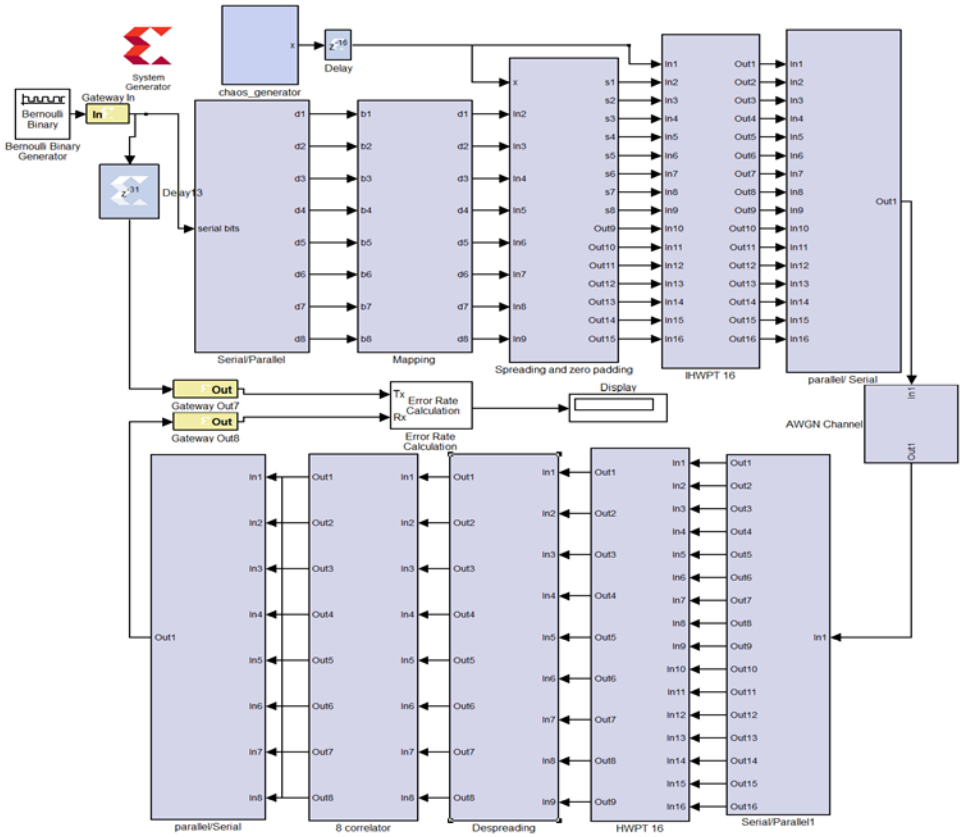

Figure 4 XSG block diagram of HWPM-DCSK transceiver system

Table 1 Implementation parameters of the HWPM-DCSK system

Input Data	Bernoulli binary signal generator Format: Output data type is double
Chaos generator	Chebyshev polynomial function $x_{k+1} = 1 - 2x_k^2$ Format: fixed point signed 2's complemented
Mapping	BPSK Format: fixed point signed 2's complemented
Spreading factor(β)	4
Number of the subcarrier	16
Number of input bits	8
Channel model	AWGN

4.1Transmitter section

In this section source input, chaos signal generator, serial to parallel, mapping, spreading and zero padding, IFHWPT and parallel to serial blocks are presented. Each block is designed using XSG in Simulink/Matlab program.

4.1.1Bernoulli binary signal generation

By using the Simulink block Bernoulli binary generator the Bernoulli binary signal has been generated. The proposed system performance is tested by using this binary data. The parameters of this block are summarized as follows: the sample time must be 1 and the type of the output data must be doubled. The gateway-in can be used to set the data to Boolean format that represents the source input to HWPM-DCSK transceiver system.

4.1.2Chaos generator block

Figure 5 shows the XSG block diagram for the chaos generator built in the XSG. The chaotic logistic map has been implemented from Equation1 that can be

used as spreading sequence. By single pulse is high voltage only at the first cycle to enter the initial value to the chaotic process and then becomes zero to select the return signal by the multiplexer during the next cycle. The type of the output data must be signed by using 24 bits of word length with 23 bits for fraction points.

4.1.3Serial to parallel converter block

The serial to parallel (S/P) block set is available in XSG library. The number of bits in the slice block is 8 and the latency is 1. The output of S/P is symbol of 8 bits to convert it into parallel bits we need slice block. The slice block is used to select a given range of bits for each input sample. The bit number in each slice is 1 and the type of the output data is unsigned. *Figure 6* shows the XSG block diagram of serial to parallel converter**.**

4.1.4Mapping block

Each parallel bit is then mapped using mapping block. This block contains eight ROM blocks. Each bit of the parallel data is must be used as addresses in the ROM block to choose one of the two phases $\{0^0, 180^0\}$, when the depth for each ROM block is [1 -1]. The type of the output data is signed. The fixed point precision has 2 bits with 0 bits for the fraction point. The delay is connected, to enable pin for each ROM block for masking all the parallel bits until it is ready for mapping. *Figure 7* shows XSG block diagram of the mapping function.

4.1.5Spreading and zero padding block

This block contains eight multipliers and the rest is zero padding. The main function of the multiplier is used for spreading by multiplying the chaotic sequence with the mapping data. The parameters of the multiplier block are summarized as follows: the type of the output data is signed, the word length of fixed point precision is 16 bits with 11 bits for the fraction points. *Figure 8* shows the XSG block diagram of spreading and zero padding blocks.

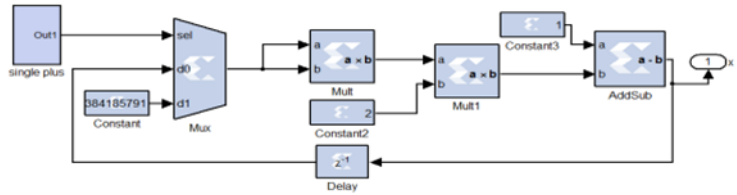

Figure 5 XSG block diagram of the chaos generator

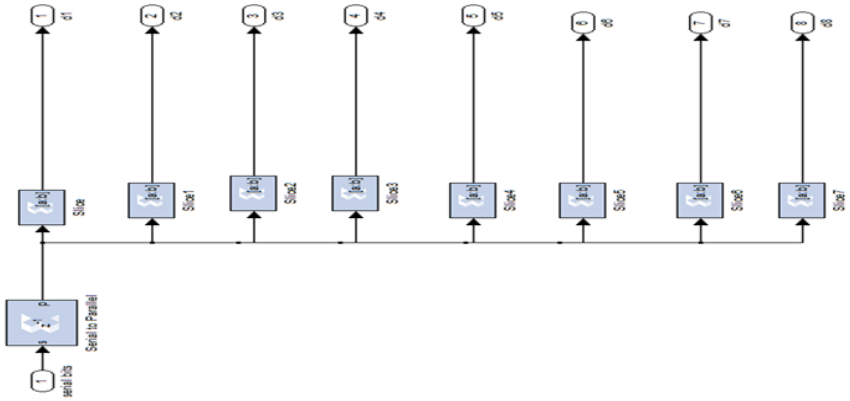

Figure 6 The XSG block diagram of serial to parallel converter

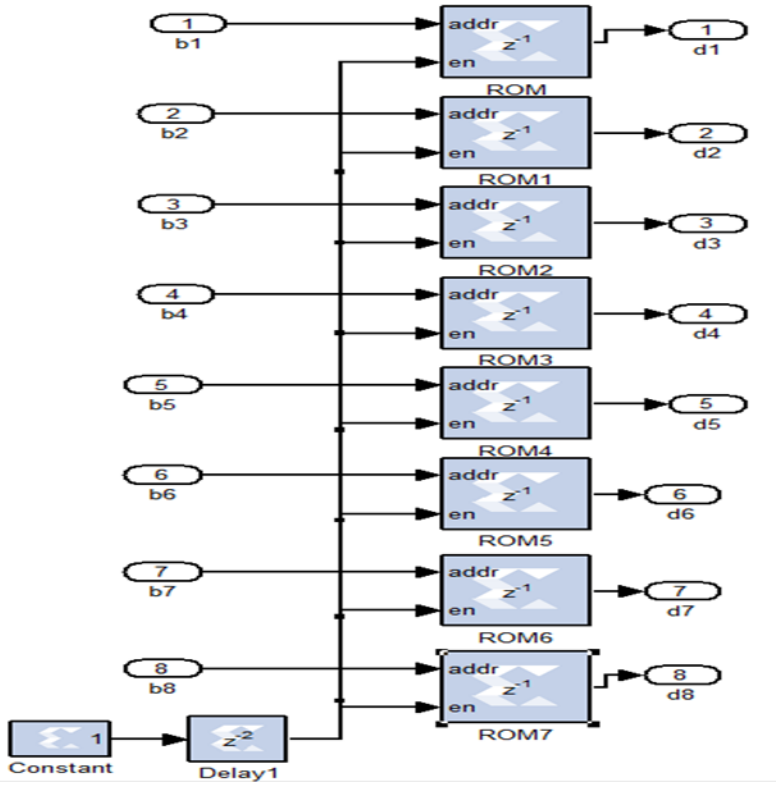

Figure 7 XSG block diagram of mapping function

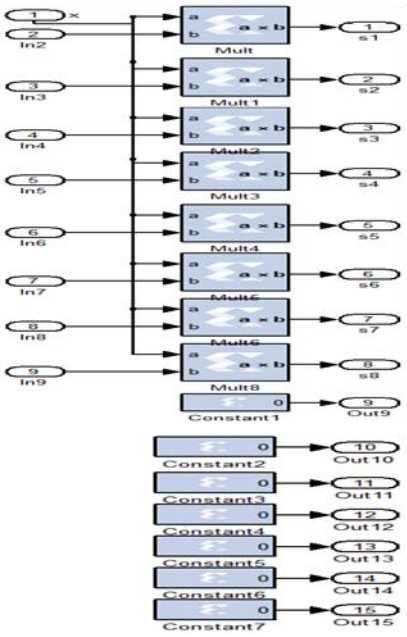

Figure 8 XSG block diagram of spreading and zero padding function

4.1.6Inverse fast wavelet packet transform

The spread signal, then passing through IFHWPT to produce the multicarrier modulated signal. IFHWPT is implemented according to the same manner as *Figure 1* but for 16 points. *Figure 9* shows the XSG block diagram of IFHWPT for 16 subcarriers. IFHWPT is used only adder and subtractor function (multiplier-less). Therefore, it is an efficient design to implement Haar WPT.

4.1.7Parallel to serial converter block

Each sample of the IFHWPT output is up-samples to 16 times using up-sampling block set. Up-sampling is is referring to the whole process in order to increase the sampling rate of multicarrier modulated signal by adding zero samples or copy the original samples between the samples to be ready used for the next step in the conversion. After up-sampling process the samples are held in latches flip flop. Linear-feedback shift register (LFSR) block is used as control signal to enable the 16 delay components. Every 16 cycles are input into the latch flip-flop. The parallel samples are then ready to enter to MUX block to multiplex in one channel.

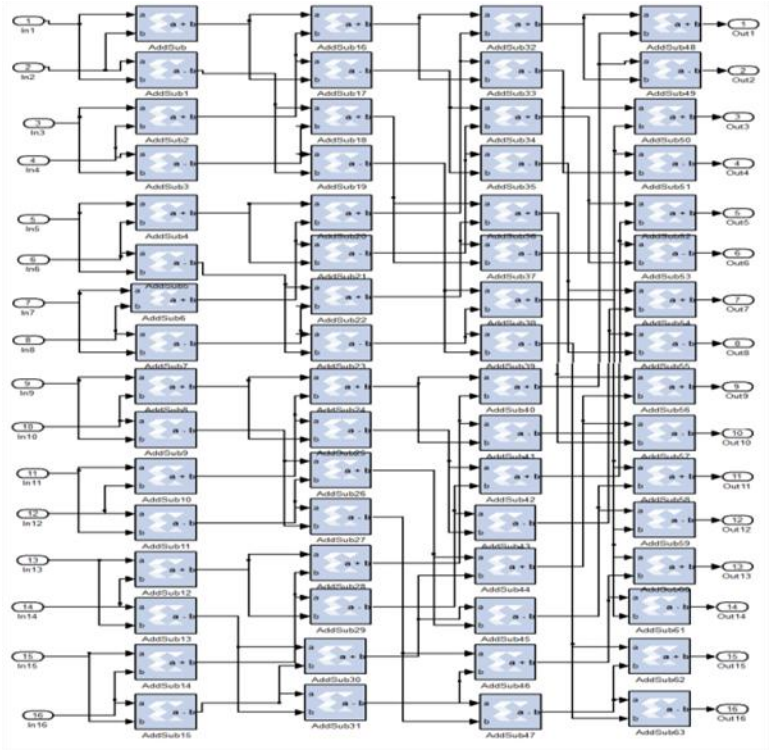

Figure 9 XSG block diagram of IFHWPT for 16 inputs

Figure 10 shows the XSG block diagram of parallel/serial converter.

AWGN block in a Simulink/MATLAB library is used to test the performance of the system. The parameters for this block are 0 dB to 20 dB for Eb/N0 (dB), the bit number per symbol is 1, 1 for input signal power and 1 S for the symbol period. *Figure 11* shows the Simulink and XSG blocks of AWGN channel.

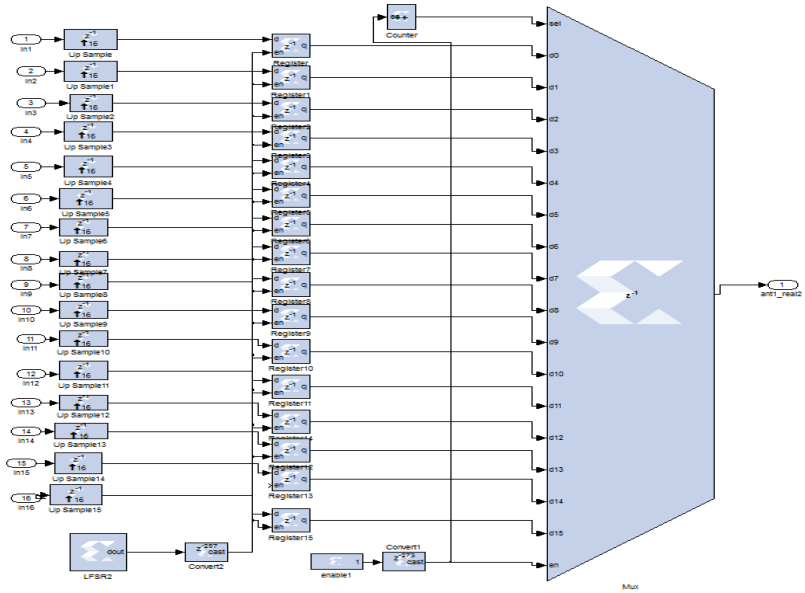

Figure 10 XSG block diagram of parallel to serial converter

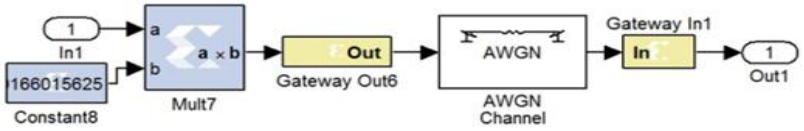

Figure 11 XSG blocks of AWGN channel

4.2Receiver section

In this section, serial to parallel converter, FHWPT, dispreading, correlator and parallel to serial converter block are presented and implemented using XSG block sets.

4.2.1Serial to parallel converter

In this block the serial sequence is converted to parallel samples using serial to parallel converter that is implemented using shift registers and then each sample is down sampled by 16 samples. *Figure 12(a)* and *Figure 12(b)* shows the XSG for the serial /parallel block.

4.2.2Fast wavelet packet transform block

The parallel samples are then applied to FHWPT block that is used only adder and subtracted operations (multiplier-less). It is built according to *Figure 1* but instead of 8 inputs becomes 16 inputs. *Figure 13* shows the XSG for this block.

4.2.3Despreading

This block built from eight multipliers and the main function of the despreading block is the reverse function of the spreading block. The parameters of the multiplier block are followed; the output data type is signed, the fixed point precision with 16 bits of integer and 11 bits for a binary point. *Figure 14* shows the XSG for this block.

4.2.4Correlator block

The correlator block is used to perform the correlation process between the data chaotic sequence and the chaotic reference signal. The correlator block is built from 8 subsystems. Each subsystem is built by using 8 shift registers and relational Xilinx block. The output from each shift register is input to add-sub block. In each subsystem must be used 7 add-sub blocks. The enable bin in add-sub block must be used to indicate for starting to read the parallel data simultaneously. Then the signal is obtained by parallel add-sub operations are compared with the constant, when the constant value is zero by using relational Xilinx block. The relational block performs the demapping process for the parallel data. *Figures 15(a)* and *Figure 15(b)* show the correlator XSG block.

4.2.5Parallel to serial converter

It is used to convert the parallel demapping samples to serial samples. This block isn't available in the Simulink library. It is built from 16 flip-flops, delay, pattern, counter and multiplexer Xilinx blocks. By activating the enable pin the 16 samples have been latched to the 16 flip-flops, and then the multiplexer has been used to extract one sample at a time depending on counter assignment. The delay here is used for synchronization. The LFSR is used to make a pattern for storing the complete sample. *Figure 16* shows the XSG for parallel to serial converter.

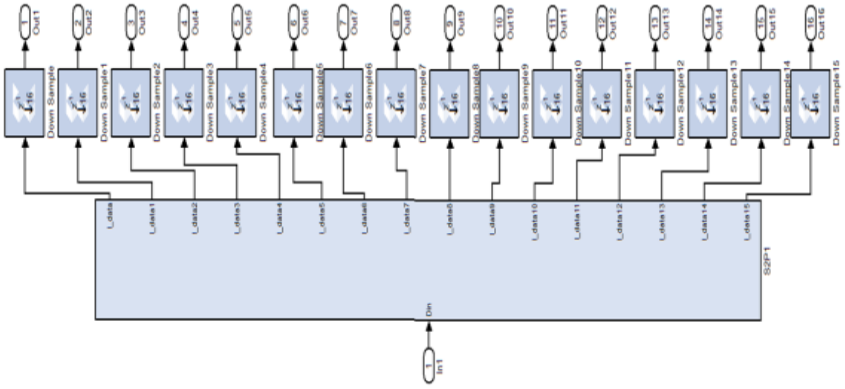

Figure 12(a) XSG for serial/parallel block

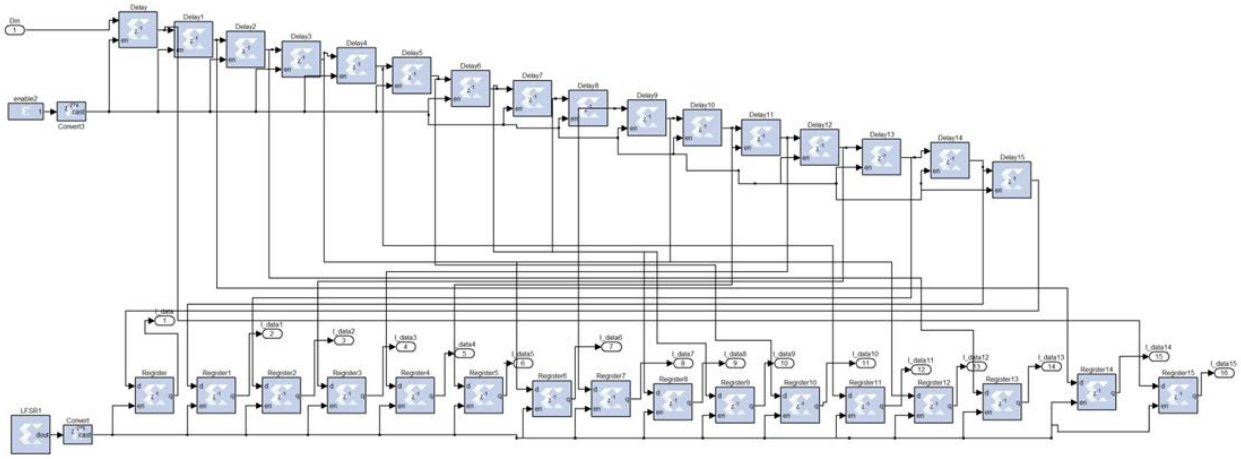

Figure 12(b) S2P XSG block

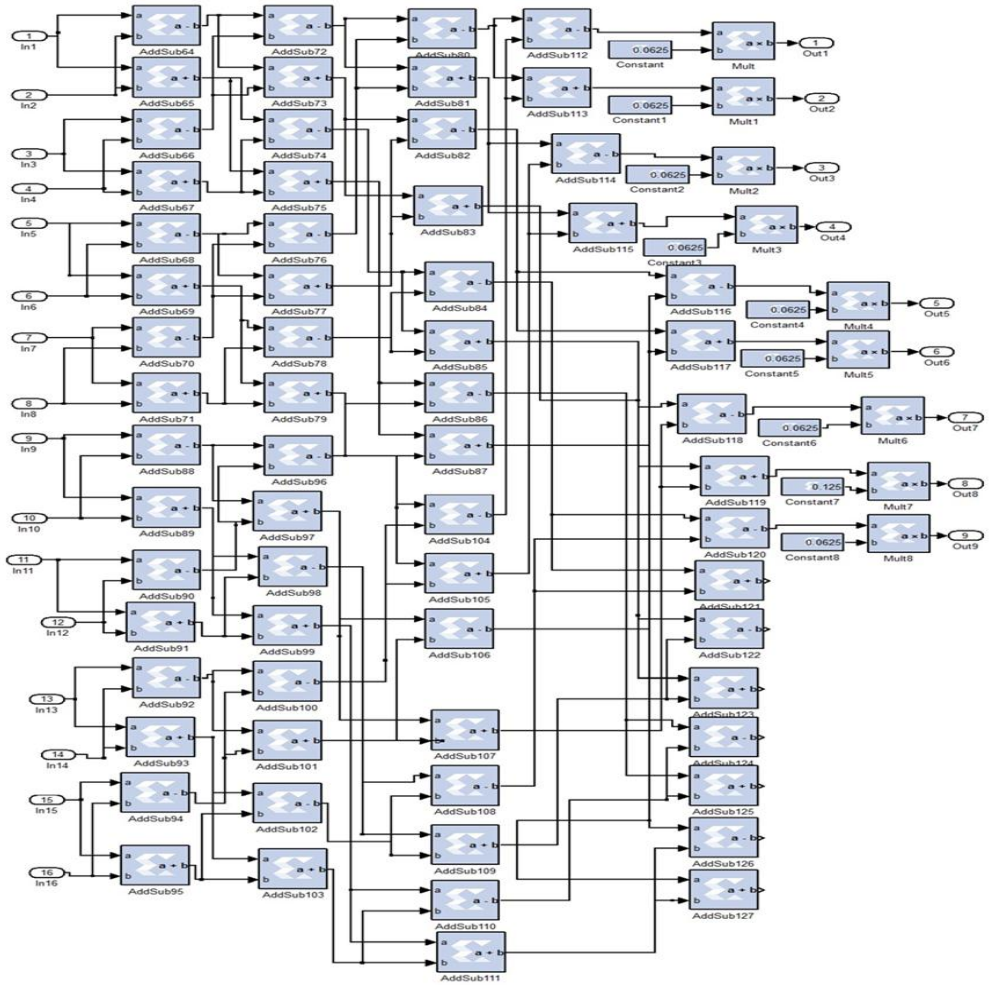

Figure 13 Xilinx system generator for the HWPM

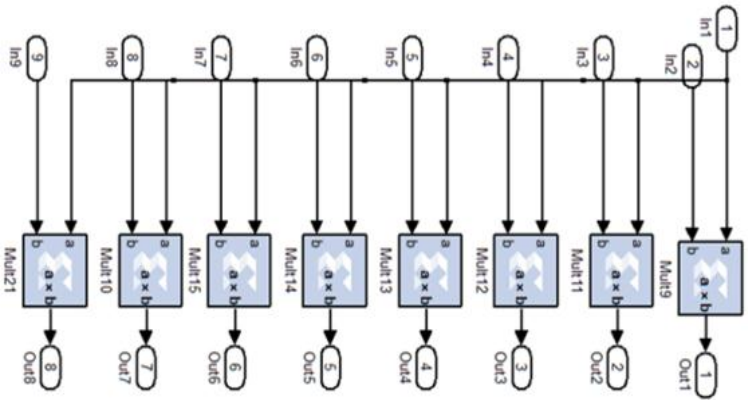

Figure 14 XSG for the despreading block

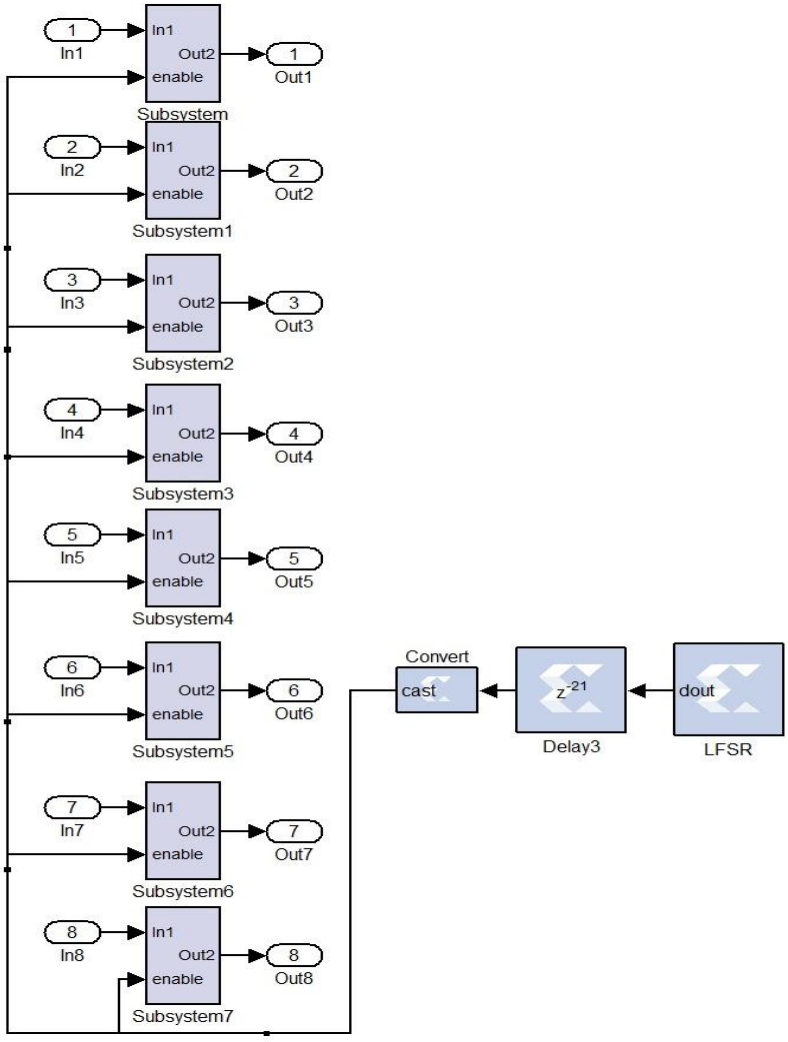

Figure 15(a) Correlator Xilinx system generator block

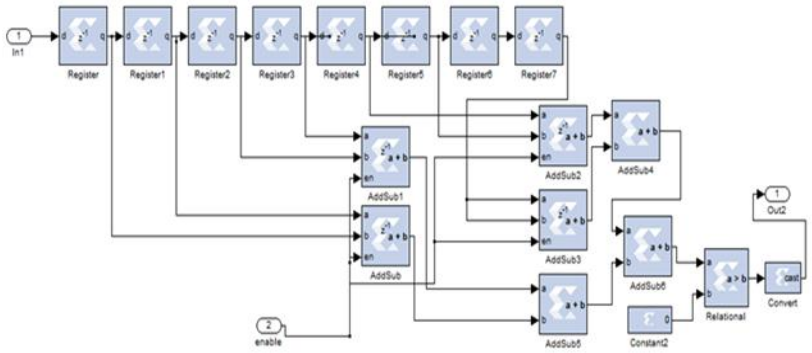

Figure 15(b) The subsystem (Correlator XSG block)

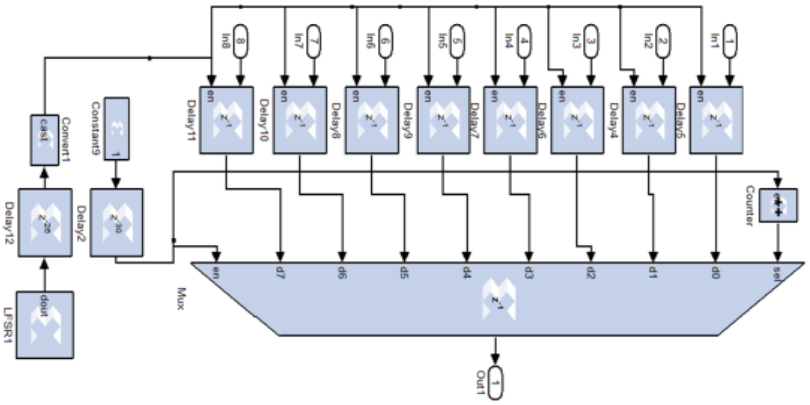

Figure 16 The Xilinx system generator for parallel/serial block

5.Xilinx system generator simulation results and discussion

The result waveforms show the outputs of every part of the WPM-DCSK system. It is performed by using XSG. It has been plotted through MATLAB program. In the WPM-DCSK system, the number of parallel bits is 8 and the subcarrier number is 16. The spreading factor (β) is 4. *Figure 17* illustrated the XSG waveform simulation of the serial to parallel block. The bit rate for serial data entered to the serial to parallel block is 100Mbps, when the data is output parallel. The rate of the parallel data is decreased to 12.5Mbps. This means the signal contains 8 bits cycle. This signal is named sample. The 8 slices are used to output the 8 bits of each sample respectively. In this figure the output of slice 1 is appeared only.

Figure 18 illustrated the XSG waveform simulation of the mapping block. We have observed that the parallel data (b1) are mapped when the enable becomes one. The delay is connected, to enable pin for each ROM block for masking all the parallel bits until it is ready for mapping. Each 0 is mapped to -1 and each 1 is mapped to +1. *Figure 19* illustrated the XSG waveform simulation of the spreading and zero padding. In this figure, the reference chaotic signal is multiplied by the data, and then the result of multiplication is named have spread. *Figure 20* illustrated the XSG waveform simulation of the IHWPT for 16 subcarriers. *Figure 21* illustrated the XSG waveform simulation of the parallel to serial block. In this block, the multiplexer is used as time-division multiplexing (TDM). First, the parallel data is up-sampled to 16 for increase sample rate for each output sample. It has been used to extract one sample at a time depending on counter assignment. The LFSR is used to make a pattern for storing the complete sample.

With regard to the receiver side, *Figure 22* illustrates the XSG waveform simulation of the serial to parallel block. The serial data is first read and latched in flip-flop registers, when the pulse is coming to the sample is read. Each sample consists of 16 bits. Then downsampling on each read output samples to restore the previous sample rate for each sample has been performed.

Figure 23 illustrated the XSG waveform simulation of the despreading block. *Figure 24* illustrated the XSG waveform simulation of the correlator block. *Figure 25* illustrated the XSG waveform simulation of the parallel to serial block. The multiplexer has been used to extract one sample at a time depending on counter assignment. The delay here is used for synchronization. The output data is serial. *Figure 26* illustrated the XSG waveform simulation of the comparison between the transmitted signal and the received signal. *Table 2* illustrated the comparison between the bit error rate (BER) simulation and BER in FPGA, so the BER in the simulation is matched roughly to the BER in FPGA.

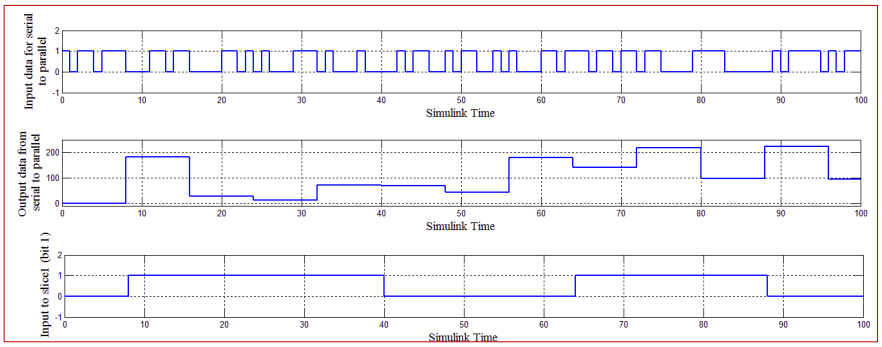

Figure 17 Xilinx system generated waveform simulation of the serial to parallel block

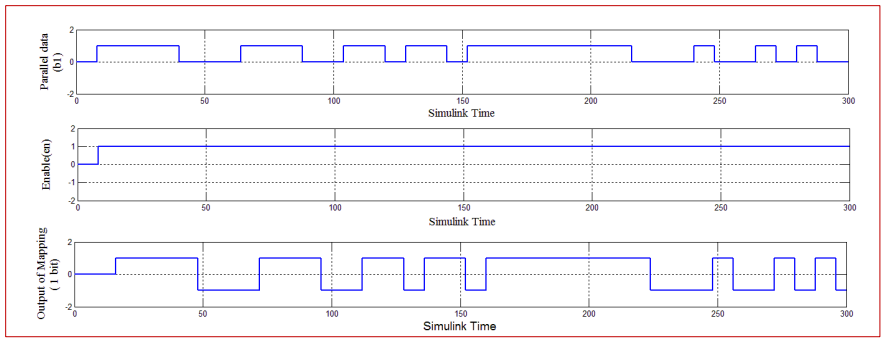

Figure 18 Xilinx system generated waveform simulation of the Mapping block

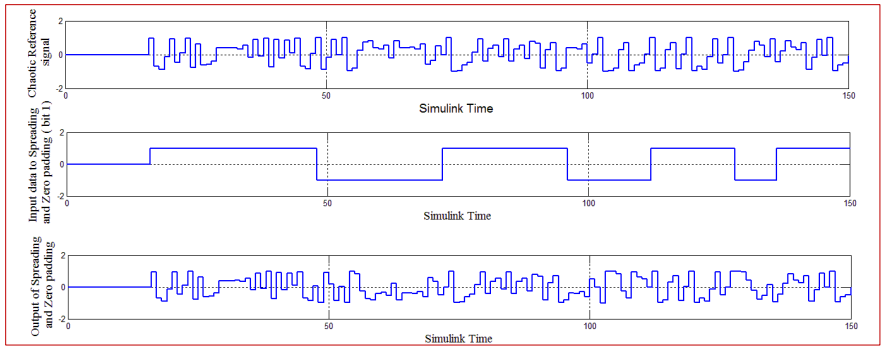

Figure 19 Xilinx system generated waveform simulation of the spreading and zero padding block

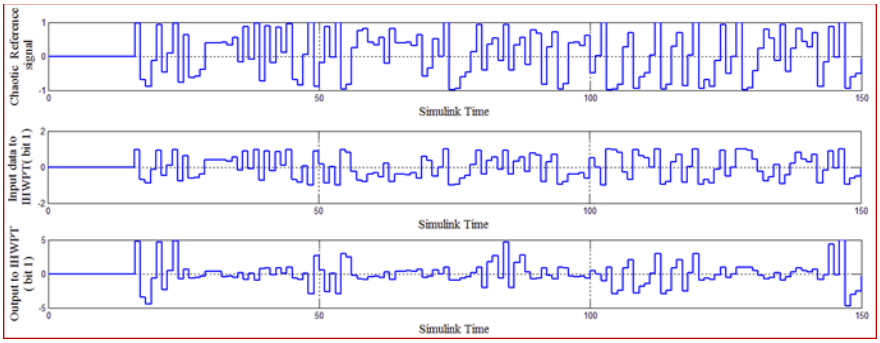

Figure 20 Xilinx system generated waveform simulation of the IHWPT block

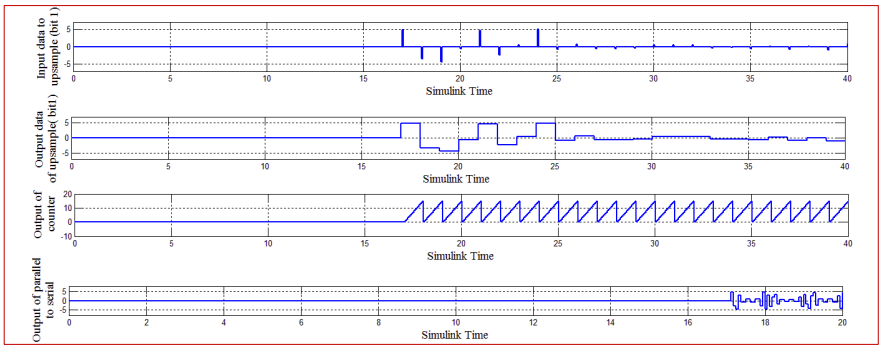

Figure 21 Xilinx system generated waveform simulation of the parallel to serial block

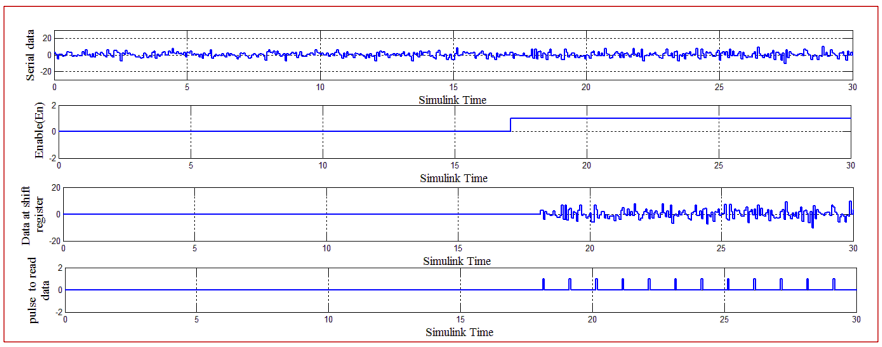

Figure 22 Xilinx system generated waveform simulation of the serial to parallel block

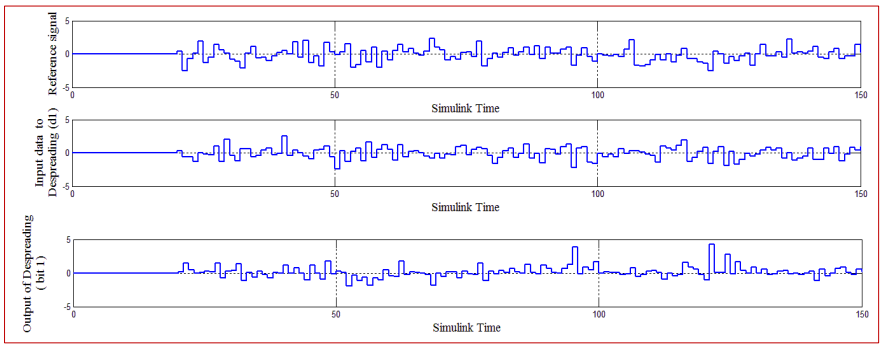

Figure 23 Xilinx system generated waveform simulation of the despreading block

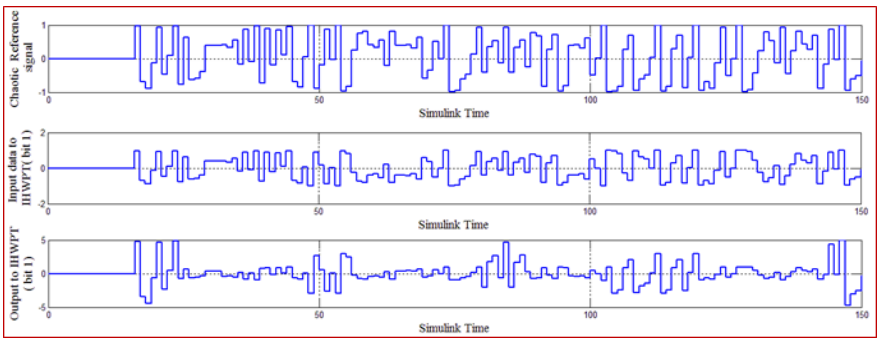

Figure 24 Xilinx system generated waveform simulation of the corellator block

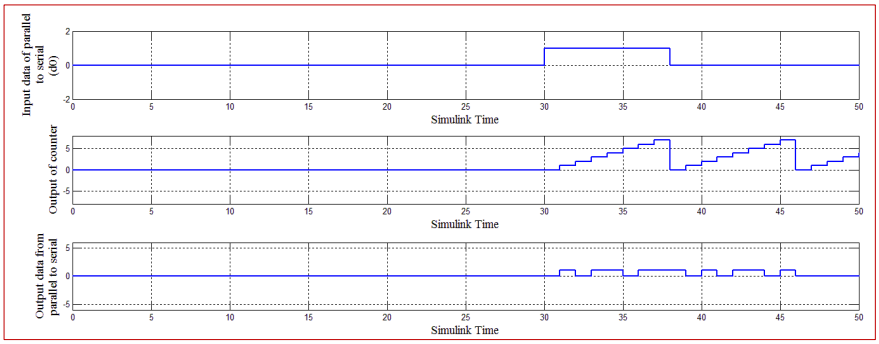

Figure 25 Xilinx system generated waveform simulation of the parallel to serial block on the receiver side

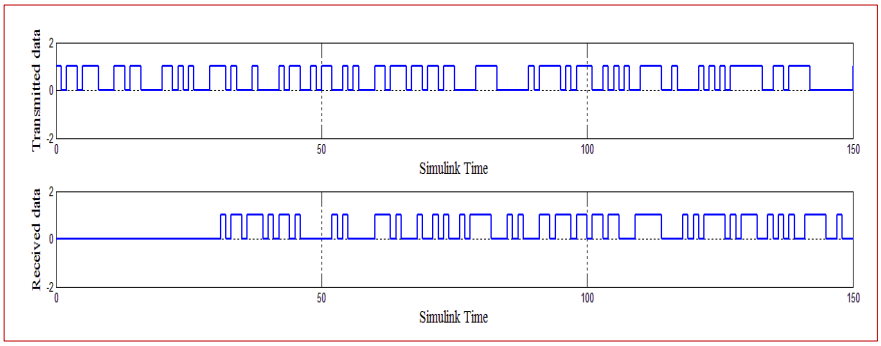

Figure 26 Xilinx system generated waveform comparison between the transmitted and the received data

Table 2 The comparison between the BER in simulation and FPGA under AWGN channel

Signal-to-noise ratio (SNR) (dB)	BER simulation	BER FPGA
0	0.2788	0.2679
1	0.2587	0.2379
2	0.2300	0.193
3	0.1863	0.1531
4	0.1363	0.1098
5	0.0737	0.07488
6	0.0688	0.04493
7	0.0187	0.02329
8	0.0125	0.009983
9	0.0037	0.004992
10	0	0.003328

6.Synthesis reports

Bit stream file or VHDL code file has been generated by Virtex 4 selections. Devices must be used for building this system. It is illustrated by ISE 14.5 program as shown in *Table 3*. The minimum period is 3.365ns and the maximum frequency is 297.155MHz.

Table 3 Device utilization summary for the HWPM-DCSK system

Device utilization summary			
Logic utilization	**Used**	**Available**	**Utilization**
Number of slices flip-flops	4,990	84,352	5%
Number of 4 input LUTs	4,682	84,352	5%
Number of occupied slices	4,511	42,176	10%
Number of slices containing only related logic	4,511	4,511	100%
Number of slices containing unrelated logic	0	4,511	0%
Total number of 4 input LUTs	4,974	84,352	5%
Number used as logic	4,581		
Number used as a route-thru	292		
Number used as shift registers	101		
Number of bonded IOBs	276	576	47%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Number of FIFO16/RAMB16s	8	376	2%
Number used as RAMB16s	8		
Number of DSP48s	113	160	70%
Average fanout of non-clock nets	1.82		

7.Conclusion

The HWPM-DCSK system has been designed and implemented successfully by using XSG. Software tools represented by Xilinx ISE version 14.5 and Xilinx Virtex 4 (xc4vfx100-12ff1152) board are used in the implementation. The results that are obtained by the hardware simulation prove this system works in correct form. The real time operations are supported by the synthesis results. Furthermore, with AWGN, the results show that the detected signal at the receiving side is similar to that of the original transmitted signal. The future work includes the study and test HWPM-DCSK proposal system by the hardware co-simulation.

Acknowledgment

None.

Conflicts of interest

The authors have no conflicts of interest to declare.

References

[1] Kaddoum G. Wireless chaos-based communication systems: a comprehensive survey. IEEE Access. 2016; 4:2621-48.

[2] Kaddoum G, Chargé P, Roviras D, Fournier-Prunaret D. Performance analysis of differential chaos shift keying over an AWGN channel. In international conference on advances in computational tools for engineering applications 2009 (pp. 255-8). IEEE.

[3] Kaddoum G, Gagnon F, Richardson FD. Design of a secure multi-carrier DCSK system. In international symposium on wireless communication systems 2012 (pp. 964-8). IEEE.

[4] Kaddoum G, Richardson FD, Gagnon F. Design and analysis of a multi-carrier differential chaos shift keying communication system. IEEE Transactions on Communications. 2013; 61(8):3281-91.

[5] Li S, Zhao Y, Wu Z. Design and analysis of an OFDM-based differential chaos shift keying communication system. Journal of Communications. 2015; 10(3):199-205.

[6] Hasan FS. Design and analysis of an OFDM-based short reference quadrature chaos shift keying communication system. Wireless Personal Communications. 2017; 96(2):2205-22.

[7] Kaddoum G, Richardson FD, Adouni S, Gagnon F, Thibeault C. Multi-user multi-carrier differential chaos shift keying communication system. In international conference on wireless communications and mobile computing 2013 (pp. 1798-802). IEEE.

[8] Kaddoum G, Shokraneh F. Analog network coding for multi-user multi-carrier differential chaos shift keying communication system. IEEE Transactions on Wireless Communications. 2015; 14(3):1492-505.

[9] Kaddoum G. Design and performance analysis of a multiuser OFDM based differential chaos shift keying communication system. IEEE Transactions on Communications. 2016; 64(1):249-60.

[10] Yang H, Tang WK, Chen G, Jiang GP. Multi-carrier chaos shift keying: system design and performance analysis. IEEE Transactions on Circuits and Systems I: Regular Papers. 2017; 64(8):2182-94.

[11] Jamin A, Mähönen P. Wavelet packet modulation for wireless communications. Wireless Communications and Mobile Computing. 2005; 5(2):123-37.
[12] Wang S, Zhu J, Zhou J. OFDM-based chaotic spread spectrum communications with high bandwidth efficiency. In international conference on control engineering and communication technology 2012 (pp. 940-3). IEEE.
[13] Sayed WS, Radwan AG, Rezk AA, Fahmy HA. Finite precision logistic map between computational efficiency and accuracy with encryption applications. Complexity. 2017:1-21.
[14] Liu Z, Zhang J, Liu H. Design of the differential chaos shift keying communication system based on DSP builder. Computer Modelling & New Technologies. 2014; 18(12c):138-43.
[15] Abdullah HN, Sahib F, Valenzuela A. Design of high speed Haar wavelet packet modulation (HWPM) system. In proceedings of mosharaka international conference on communications, computers and applications 2011 (pp. 65-72).
[16] Abdullah H, Hassan F, Valenzuela A. FPGA based fast complex wavelet packet modulation (FCWPM) system. In international conference on circuits and systems 2013 (pp. 114-9). IEEE.
[17] Hasan FS. FPGA based 2× 2 MMSE MIMO-OFDM system using Xilinx system generator. Journal of Engineering and Sustainable Development. 2018; 21(1):152-77.
[18] Ganesh GV, Krishna BM, Kumar KS, Prathyusha T, Venkatesh R, Jessy TV. FPGA implementation of OFDM transmitter using Simulink and Xilinx system generator. Journal of Theoretical and Applied Information Technology. 2015; 78(1):125-31.

Rawaa Abed Mohammed was born in Baghdad, Iraq in 1986. She received her B.Sc. degree in Computer Engineering Techniques from Electrical Engineering Technical College, Middle Technical University, Baghdad, Iraq in 2007. Her recent research activities are Wavelet based DCSK, FPGA and Xilinx System Generator based Communication System.
Email: rawaa.abed.m@gmail.com

Fadhil S. Hasan was born in Baghdad, Iraq in 1978. He received his B.Sc. degree in Electrical Engineering in 2000 and his M.Sc. degree in Electronics and Communication Engineering in 2003, both from the Mustansiriyah University, Iraq. He received Ph.D. degree in 2013 in Electronics and Communication Engineering from the Basrah University, Iraq. In 2005, he joined the faculty of Engineering at the Mustansiriyah University in Baghdad. His recent research activities are Wireless Communication Systems, Multicarrier System, Wavelet based OFDM, MIMO System, Speech Signal Processing, Chaotic Modulation, FPGA and Xilinx System Generator based Communication System. Now he has been an Assistant Professor at the Mustansiriyah University, Iraq.
Email: Fadel_sahib@uomustansiriyah.edu.iq

Dr. Mohammed Joudah Zaiter received his B.Sc. in Electrical and Electronics Engineering/Computers and M.Sc. in Electrical Engineering from the Al-Rasheed College of Engineering and Science, University of Technology, Baghdad, Iraq in 1992 and 2004, respectively. He received his Ph.D. in Communication Engineering, Universiti Tenaga Nasional (UNITEN), Malaysia 2014. He is currently working as a Lecturer in Computer Engineering Techniques Department, Electrical Engineering Technical College, Middle Technical University, Iraq**.** His research interests are focused on High Performance and Energy Efficiency of the Wireless Communication Systems and Optical Communication Networks.
Email: mjzaiter@eetc.mtu.edu.iq