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Research Article

Multi-objective predictive control for three-phase three-level neutral-point clamped inverter

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Abstract
This paper describes the strategy for the implementation of model predictive control (MPC) to a three-phase multilevel inverter. Though MPC has been active since the 1960s, it has only gained traction in recent years owing to the increased processing capabilities of modern devices which now help to remove the obstacle of large delays in this scheme. Moreover, this method is far superior in control of multiple input multiple output systems, could handle constraints of operation, and removed the necessity of a modulator, which was required in the popular pulse width modulation technique (PWM). In this paper, to achieve this scheme, we developed a novel cost function to reduce distortions in current output along with switching frequency reduction and capacitor voltage balancing. This was achieved by the iterative nature of the MPC that provides the least error which was then implemented in the next step. The action of prediction for the MPC was further tuned by adjusting the sampling time. In the process of implementation of MPC, the mathematical model of the converter and load was developed and simulations were performed on MATLAB/Simulink to understand the effect of changing the weighting factor on the system response. In this manner, this paper demonstrated the degree of control over DC-link capacitor voltages and switching frequency. The merit of such a predictive control over conventional PWM-based proportional integral (PWM-PI) control was analyzed by comparing the distortions in their respective waveforms and dynamic responses. It is observed that our strategy is more effective in reference tracking and gives a faster dynamic response as compared to PWM-PI control. Also, MPC was implemented using Intel's DE0-Nano board, a field programmable gate array (FPGA) platform, and the results were analyzed to prove the feasibility of the strategy for field use.

Keywords
Least square method, Model predictive controller, Multi-objective control, MATLAB, Neutral point clamped inverter.

1.Introduction
In recent years, multilevel inverters (MLIs) have proved to be the most attractive technology because of their exceptional features as proposed in [1]. Such type of inverters produces several levels of output voltage or current which can be approximated to the desired waveform by introducing an appropriate number of steps. A conventional three-phase two-level inverter has the disadvantage of operating at high switching frequencies. As a consequence, the switching losses are high and compensation is to be made by opting for lower component ratings. Moreover, issues such as electromagnetic interference, harmonic distortions, and large change in voltage with time are common.

In recent years, the industry has seen an increase in the power demand which now reaches the megawatt level. Because of the aforementioned issues, integration of such power electronic converters directly into high-voltage grids is challenging [2].

In contrast, MLIs differ in their structural composition and thus are better suited to produce high-power, high-voltage outputs [3, 4]. Greater power ratings can now be simply achieved by increasing the voltage levels, eliminating the need to compromise on the ratings of the component. Thus, MLIs are used as a solution for working with higher voltage levels.

The greater the number of steps in the waveform, the lesser would be the harmonic content in it, as it would be approximated to an ideal sinusoidal

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waveform. The most used topology of MLIs is diode clamped structure because of low switching frequency and less power consumed by semiconductors as illustrated in [5]. These inverters tend to be suitable for medium voltage applications like acoustic and pumping requirements for residential areas and other general motor drive applications [3, 6].

However, this topology suffers from issues like commutation losses and poor quality of current at the output. Furthermore, the divergence of averaged neutral currents from balanced values results in the generation of neutral point voltage [7]. In fact, this phenomenon becomes more apparent as the voltage levels are increased beyond four, resulting in difficulties in adopting this topology.

Existing literature states multiple control methods to deal with the above-mentioned issues which include hysteresis control, pulse width modulation (PWM) with proportional integral (PI) control, etc. [8]. However, their applications are limited to low-power areas because of various problems as mentioned in [9–14]. Model predictive control (MPC) triumphs over conventional methods and can be applied as it can handle constraints and nonlinearities in the model and covers a wide range of multiple input and multiple output systems. Use of a finite control set (FCS) MPC removes the necessity of a modulator [9]. The design of a suitable cost function is also important for the MPC to achieve the desired control objective [15]. Digital signal processor (DSP) based implementations are most common in literature for the MPC. However, it introduces a relatively large time delay which can be reduced using a field programmable gate array (FPGA) [16]. The design of a suitable cost function is also important.

Our proposed idea comprises the working of FCS-MPC for three-phase three-level inverters and optimizing its performance by a novel cost function. Capacitor voltage balancing and reduction in switching frequency are considered for the cost function. Reduction in switching frequency is crucial as it indicates the reduction of commutation losses by switching to the desired value in the least possible steps. Therefore, we will further compare MPC against classic PWM-based proportional integral (PWM-PI) control as part of the analysis with a generalized algorithm and the determination of parameters. The analysis is conducted using simulations on MATLAB/Simulink software. They are evaluated based on specifications including structural development, total harmonic distortions (THD), ease in realization, and other standards, which will be defined more clearly in upcoming sections. Intel's DE0-Nano board, an FPGA platform, is used for the parallel implementation of all the iterative calculations in MPC to reduce the time delay.

In this paper, section-2 discusses the literature corresponding to related work. Section-3 explains the methods employed for the development of MPC for a three-phase three-level neutral-point diode clamped inverter. The functions of diode-clamped MLIs and their functioning with an MPC scheme are explained in this section which includes modeling of the inverter, design of cost function, weighting factors, etc. The results are shown in comparison with conventional control methods and various parametric variations are shown in section-4. Section-5 analyses and discusses the result with its limitation and possible solution. Conclusions and future work are explained in section-6.

2.Literature review

Various control strategies such as hysteresis control and linear PI controller with PWM are explained in detail in [7, 8]. Hysteresis control can improve the quality of the current and is easy to implement however, the switching losses associated with the variable frequency restrict the use of hysteresis control to low power applications [8].

Adding linear control with PWM is the most popular control technique of which the most common is level-shifted phase disposition PWM. Space vector-based PWM can also prove to be an alternate solution to balance the neutral point voltages over a wide range of modulation indices and power factor as proposed in [9, 10]. In these methods, a voltage vector can be generated by multiple switching states, thereby eliminating neutral current over the period of control. Similar extrapolation is realized by a carrier overlapped PWM in [11] for the neutral point clamped (NPC) Inverter.

Voltage balance can also be achieved by other control methods such as nearest-three-vectors modulation as shown in [1, 12–14]. However, as we increase the voltage levels of the inverter, voltage balance is lost when applied to applications that span a full range of modulation indices and power factors.

Predictive control technique becomes popular because of the development of fast computing

techniques [16]. Various predictive control methods are available in the literature and it is documented well in [6]. The vital feature of predictive control should be its flexibility with linearities/non-linearities of the structure and estimating the state of controlled variables for the next instant [16, 17]. When dealing with power electronics, MPC can be divided into two groups based on the need for a modulation stage [18]: FCS-MPC and continuous control set (CCS) MPC. The latter uses a sinusoidal PWM or space vector modulator to generate switching states [19, 20]. The former, on the other hand, uses a discrete model to instantly predict the value of the control variable, and switching action which would reduce the cost is applied in the next instant [21, 22].

The property of CCS-MPC to accommodate nonlinearities was exploited in [23, 24] where it was used to reduce the frequency of switching for the inverter by evaluating the error in current corresponding to each switching state. Another approach, which utilizes the important feature of FCS-MPC to directly apply the control action to the converter switches without the need for a signal modulator is presented in [9, 25–27]. This in turn improves the response of the system to internal and external dynamics on the cost of the computational burden. An FCS-MPC strategy to reduce the midpoint voltage fluctuations for the three-phase three-level inverter with fixed switching frequency is explained in [25] whereas a DSP-based-MPC strategy is implemented in [26]. Using the technique in [25], the dynamic performance is improved but the sampling frequency required is large. The author in [27] also explains a DSP-based FCS-MPC strategy but for the control of a single phase split source inverter for the standalone PV system.

In recent years, there has been a growing trend of reducing the number of sensors employed, energy spent on control signals, and the complexity of the communication networks as they benefit the manufacturer by reducing the implementation and computational cost. MPC by its nature has a very high computational burden which has been known to cause an increase in the hardware requirements for physical implementation. Elimination of redundant voltage vectors to reduce the computation as proposed for H-bridge MIs [28] serves as the motivation for manually removing redundant voltage vectors from the model in this paper.

Using MPC, the desired control objective can be achieved by designing a suitable cost function [29, 30] which leads to the crafting of our novel cost function which reduces the switching frequency and balances the capacitor voltages along with the current harmonic reduction. The weights need to be selected according to the requirement of the application and are generally tuned using heuristic methods. The author in [29] presents one such method of using a branch and bound algorithm for zeroing in on the appropriate weight. Such manually tuned weights are not robust and might fail to respond to faults. In [30] an automatic tuning method of tuning weights is presented, which is tuned with every sampling instant. A fuzzy-based tuning method is presented in [31] to adjust the weight of the MPC to reduce the steady-state oscillations which can be generated due to the mismatch of the parameters of the MPC with the real system. A computationally heavy method using particle swarm optimization is presented in [32, 33] but using such a method would limit the robustness of MPC by reducing its bandwidth.

The most common implementation of MPC is using a DSP to perform the iterative calculations, given the ease of coding with programming languages like C/C++, and then using an FPGA for implementing the commutation [34]. In addition to the complexity of using two different digital control devices, the use of serial computing using DSP for iterative calculations introduced relatively large time delays to the process. Because of the parallel computing nature of FPGA, various applications are reported in the literature in which the MPC computations are made faster using FPGA [35–37]. An FPGA-based controller for matrix inverter is implemented in [16], which serves as the motivation for this paper to fully parallelize all the iterative calculations. The author in [38] also analyzed the effectiveness of FPGA-based MPC for direct matrix converters by utilizing its pipelining capability. The technique to reduce the MPC computational burden on FPGA using finite word length is explored in [39].

The use of high-level synthesis for the implementation of MPC on FPGA [40] for applications such as autonomous driving [41], two-dimensional-crane [42], robotics, etc. is also analyzed by many researchers in addition to its acceleration capability. FPGA-based permanent-magnet synchronous motor (PMSM) drive system using FSC-MPC is implemented in [43], in which the FPGA code is generated in integration with MATLAB/Simulink to reduce the effort for system development. In recent years, researchers [44–46] have further explored the possibility of integrating

deep neural networks with MPC for reducing its computational efforts for the advanced control of highly nonlinear power electronic converters.

These ideas lead to the proposed implementation of FSC-MPC for the current control of three phase three-level diode-clamped inverter with a novel cost function. It balances the capacitor voltages and also reduces the switching frequency in addition to the reduction in current distortion. The iterative computation is parallelized using FPGA to reduce the overall latency in computation.

3.Methods

This paper employs MPC for a three-phase three-level NPC inverter working for a star-connected balanced resistor-inductor-back emf. (RLE). The discrete-time model for predictions and techniques in reducing the cost function to realize the system's optimum performance are also discussed in this paper. In the optimization process, we focused on capacitor voltage balancing and switching frequency reduction methods, including the estimation of the weighing factor. This methodology section first describes the overview of the NPC three-level inverter, MPC, and the factors that need to be considered for the implementation of MPC-based NPC. The next subsection describes the modeling of MPC-based NPC which includes the modeling of inverter, load, and the MPC with a novel cost function that takes care of both capacitor voltage balancing and switching frequency reduction. The next subsection describes the algorithm for implementation and then the strategies for the implementation using FPGA.

3.1NPC three-level inverter

The inverter as shown in *Figure 1* consists of semiconductor switches and two parallel connected capacitors C1 and C2, which are primarily responsible for supplying a split 3-level DC stiff voltage from the DC bus. These capacitors are responsible for different DC levels in output waveforms. The neutral point is defined as the connection of the two DC capacitors.

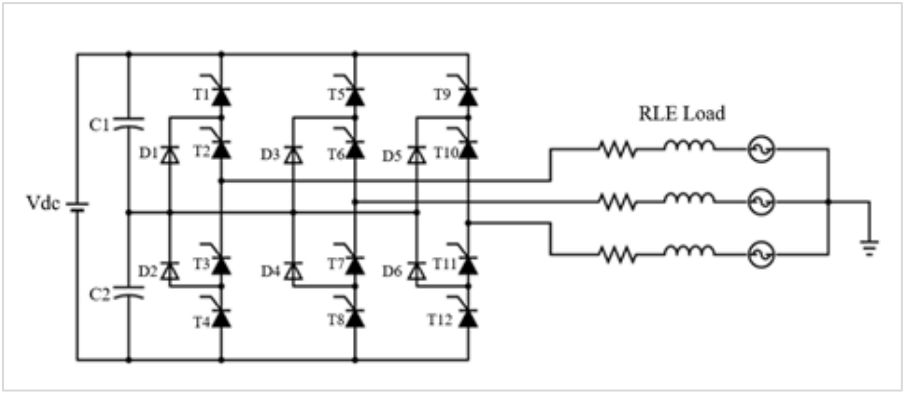


Figure 1 Three phase three-level NPC inverter

The circuit is distinguished from the conventional two-level inverter by connecting clamping diodes across the switches, which in effect, cut the switch voltage to half the value of the DC bus voltage level. As such, we obtain three feasible states in this topology: 0, +Vdc/2, and -Vdc/2; with two pairs of complementary switches in each phase. Say, the inverter is X level. Then in such a structure 2(X-1) switching components would be required, where (X-1) switches are ON simultaneously, and (X-1) number of capacitors are required in the inverter circuit along with (X-1)×(X-2) number of diodes. The output waveforms generated by these converters have much lower harmonic content, and it is economical to consider its application compared with other multilevel topologies.

3.2Model predictive control (MPC)

In power converters, the processes due to switching actions are usually nonlinear, and MPC can solve linear as well as nonlinear systems. This property of MPC helps in dealing with complicated systems with ease. Inherent constraints and restrictions of a system for security reasons can be incorporated within the MPC algorithm as well. The paper also discusses the performance of controllers with parametric variations which helps to understand their proper choice.

In the context of this paper, the 27 switching states of the three-phase three-level inverter presented a basis on which the prediction of the inverter behavior depends. Moreover, to achieve optimal control, it was necessary to optimize the control variables using an optimization technique. Thus, in addition to requiring a mathematical model of the inverter, we would need to define a function of control variables to be optimized. Before stepping into these designing processes, it helps to understand how control is achieved in this scheme.

The most crucial step is understanding the desired behavior of the system and operating on the control variables via a cost function in such a manner as to realize the aforementioned requirements. This function could consider reference values, future predicted states, and future actuations as its parameters as given by Equation 1.

$$J=f(x(k), u(k),\ldots..u(k+M)) \quad (1)$$

Here J represents the cost function, M is the prediction horizon and k is the next instant. States and actuations are represented with 'x' and 'u' respectively. Further, we solve the optimization problem consisting of the previously defined cost function J, a range of instances that are now called 'Prediction Horizon' in time as M, which is subject to the complexity of the process model. Upon solving the cost function, we obtain a sequence of M actuations, of which the controller implements only the first of the set, while the rest serve as the basis of fine-tuning. In the case of a unity prediction horizon, the controller chooses the actuation corresponding to the least value in the solution vector.

As shown in *Figure 2*, in implementing MPC, the first step is to create the system model. Past and current values of the control variables along with the estimated future control actions were estimated based on the mathematical model of the system. Thus, the greater the accuracy with which the dynamic behavior of the system is represented in the model, the better the accuracy of the control actions. Yet, the model should be simple enough to be implemented and understood by other professionals.

The next fundamental part of the control is the optimizer, which delivers the control actuations. Say the nature of the cost function is quadratic, as such the optimal value is obtained as a function of estimated trajectory and past outputs and inputs. Thus, the number of variables in the cost function and the prediction horizon defines the complexity of the optimization problem, which is later compiled to give output. The MPC should follow a few primary control objectives throughout the process that we discussed above, which are:

- It should provide the slightest possible error in the controlled variable and have fast dynamic tracking and reject disturbances for given reference input.
- In case the device's power consumption is considered, it should be able to lower the losses that occur due to switching.
- Also, the control must reduce the THD of the system.

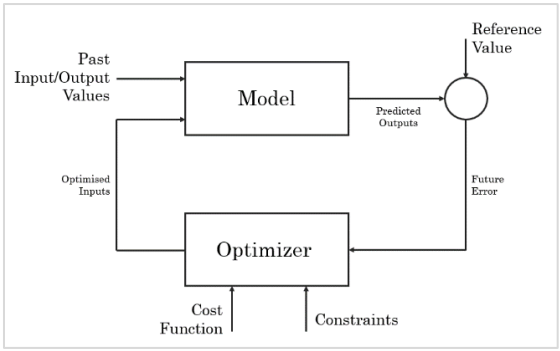


Figure 2 Basic structure of MPC

In the scope of this paper, we could see that the cost function will be used to optimize load current, dc-link capacitor voltages, and switching frequency. The control of load current was considered the primary objective and was thus given a weighting factor of one. The other subsequent terms are given a weighting factor that had been tuned using heuristic methods.

3.3 Modelling the system

An overall block diagram for the implementation is shown in *Figure 3*. This block diagram serves as a reference for the steps in modeling.

3.3.1 Inverter model

An inverter consists of many switches which are either turned ON or OFF. The state of the switches can be represented as 1 and 0 corresponding to ON and OFF respectively. The output voltage for the required leg then can be calculated using this representation. The output voltages can be related to the inverter switches mathematically as shown in *Table 1*. It is also beneficial to express this relation in S_A, S_B, and S_C for each leg, with their values taken as 1, 0, and -1 for +Vdc/2, 0, and -Vdc/2 output.

Each combination of switch states provides us with a corresponding value of voltage output possible.

These voltage values are the outputs possible for the inverter. The total number of switching states which can be obtained in the inverter is given as, $n = L^P$, L and P, are indicators of the number of levels and the number of phases respectively. In our case where we consider an NPC inverter as shown in *Figure 1*. with three levels, the total permissible switch states become 27. The DC side voltage is given as Vdc, R is the load resistance, L is the inductance, and e is the back-emf of the load.

The calculation of inverter states for single phase inverter can be completed with comparatively simpler equations. Using the Clarke transform for three-phase inverters helped to reduce the calculations.

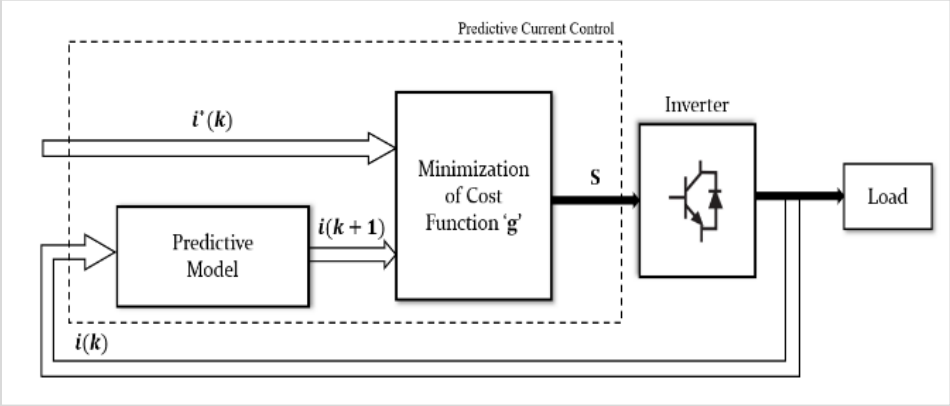


Figure 3 Overall block diagram of MPC-based inverter model

The output voltage vector is as defined in Equation 2.

$$V = \frac{2}{3}(V_{aN} + \propto V_{bN} + \propto^2 V_{cN}) \quad (2)$$

Where V_{aN}, V_{bN} and V_{cN} are the inverter output voltage of each phase and $\propto = e^{j\frac{2\pi}{3}}$ as a phase displacement of 120° degrees between the phases. They are shown as V_{xN} in *Table 1*. The voltage vectors thus calculated are then used in all further calculations.

Table 1 Relation between Switch states and output voltage

S_1	S_2	S_3	S_4	S_A, S_B, S_C	V_{xN}
1	1	0	0	1	$+V_{dc}/2$
0	1	1	0	0	0
0	1	1	1	-1	$-V_{dc}/2$

The calculation of the total output voltage vector in the orthogonal frame of reference is done with reference to *Figure 4*. Out of the 27 switch states, 9 switch states give redundant voltage vectors. Many authors suggested the mitigation of common mode voltage by removing the zero vectors, but this may increase THD. Hence, in our analysis, a zero vector is also considered, thus 19 unique switch states are obtained as shown in *Figure 4*.

3.3.2 Modelling of RLE load

The load driven by the inverter is taken as RLE as shown in *Figure 1*. For three-phase systems, the load is a star-connected RLE. Assuming the neutral of the load stays at 0V helps in the evaluation of the current for the load with the model in the controller. Kirchhoff's voltage law gives us Equation 3 for the system load for each phase as,

$$V_{xN} = L\frac{di_x}{dt} + Ri_x + e_{bx} + V_{nN} \quad (3)$$

where x represents each phase A, B, and C. L and R represent load, and V_x, e_{bx}, and i_x are voltage, back-emf, and load current vectors respectively. Equation 3 generalizes the first-order differential equations for any number of phased systems. Assuming that the neutral voltage V_{nN} is 0, the load model can be defined as a first-order differential equation which is given as Equation 4.

$$V = L\frac{di}{dt} + Ri + e_b \quad (4)$$

where V, e_b, and i are voltage, back-emf, and load current vectors respectively.

3.3.3 Estimation of parameters for the next instant

The discretization process for the sampling time T_s of the load current equation was described in this model using k^{th} sampling instant to predict the forthcoming values of measured currents and load currents from the given voltages. With several considerable discretization methods to calculate the prediction we had taken a first-order system for load modeling and by using an elementary approximation of the system's derivative, we could achieve a discrete-time

model. But this method did not help with better precision as we step up to more intricate models so a better discretization technique was needed. Forward Euler's approximation replaces $\frac{di}{dt}$ (the load derivative current) to attain a discrete expression that is flexible in predictions for a horizon instant (k+1) for the load current every twenty-seven values of V(k), a voltage vector produced by the inverter.

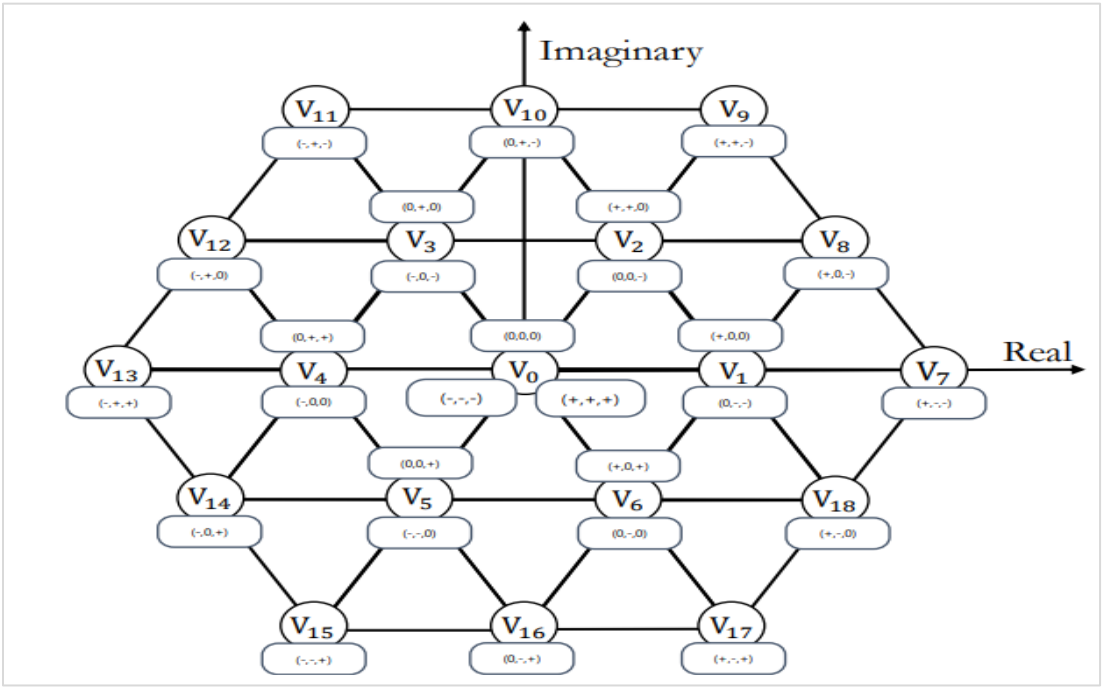


Figure 4 Three phase three-level inverter switch states

The expression is given as Equation 5.

$$i^P(k+1) = (1 - \frac{RT_S}{L})\, i(k) + \frac{T_S}{L}(V(k) - \hat{e}(k)) \quad (5)$$

where $\hat{e}(k)$ is the approximated back-emf and sampling time is T_s. The superscript 'P' indicates that the variable has the 'predicted' value. With the inclusion of load voltage and current, the estimation of back-emf can be rewritten as Equation 6.

$$e(k-1) = V(k-1) - \frac{L}{T_s}\, i(k) - \left(R - \frac{L}{T_s}\right) i(k-1) \quad (6)$$

where $e(k-1)$ is the back-emf determined at $(k-1)$. The sampling time of the controller is much smaller than the period at which the back-emf is updated, owing to its mechanical nature. Thus, $\hat{e}(k) = e(k-1)$ was assumed as there is no ample alteration in one sampling interval.

3.4 Cost function

Every possible voltage vector in *Figure 4* corresponds to a specific value of error with respect to the control variables. In order to minimize losses and to guarantee robust operation, it is important that the controller chooses the vector that would result in the least possible losses for the next instant. This is achieved by crafting a cost function J, consisting of system parameters that would be required to achieve the desired response. Generally, system variables are chosen in such a way that they follow a reference.

Control of the load current in a voltage source inverter is the most common control alternative. However, computing three phase quantities would put significant stress on the processor and lead to delays. Thus, it is more feasible to convert the quantities into orthogonal $\propto -\beta$ coordinates. In doing so, we obtain Equation 7 as a cost function:

$$J = |i_{\propto}^* - i_{\propto}^P| + \left|i_{\beta}^* - i_{\beta}^P\right| \quad (7)$$

Here the superscript 'P' represents the predicted values, $\propto -\beta$ are the orthogonal coordinates and the asterisk represents the reference values for the next instant. Moreover, the method shown above uses absolute error for computing the value of the cost function. However, in our analysis, we used the least square error method and this showed improvement in the results.

3.4.1 Capacitor voltage balancing

Capacitor voltage balancing is a necessary step for any system used in controlling the NPC since the balance of voltage across capacitors drifts away from the nominal value. Through Euler's approximation method, the dynamic behaviour of the capacitors in the next instant can be discretized using Equation 8.

$$V_c(k+1) = V_c(k) - \frac{1}{C}\, i_c(k) T_s \qquad (8)$$

Here V_c represents the capacitor voltage and i_c represents the current through the capacitor. T_s is the sampling time of the processor and the smaller the value, the greater the precision of control. However, smaller sampling periods exert an increased computational load on the processor.

Since we were already measuring the load currents, it was easier to calculate the capacitor voltages by these quantities in addition to measuring the source current. This method would further be facilitated by defining a function of switching states. For ease of programming, this function for the considered topology was defined here logically as:

```
for i = 1:27
    for j = 1:3
     Z1(j) = states(i, 2j-1) & states(i,2j)
     Z2(j) = (~states(i, 2j-1)) & (~states(i,2j))
    end
end
```

where the operator ~ performs ones-complement. Now, the current through capacitors C_1 and C_2 can be determined as:

$$i_{c1}(k) = i_{dc}(k) - Z_1(1) i_a(k) - Z_1(2) i_b(k) - Z_1(3) i_c(k)$$

$$i_{c2}(k) = i_{dc}(k) - Z_2(1) i_a(k) - Z_2(2) i_b(k) - Z_2(3) i_c(k) \qquad (9)$$

Thus, after these computations, the cost function can be modified as Equation 10.

$$J = |i_\alpha^* - i_\alpha^P| + |i_\beta^* - i_\beta^P| + \lambda_c |v_{c1}^P - v_{c2}^P| \qquad (10)$$

Here λ_c is the weighting factor for the capacitor voltages. Weights and their choice are explained in Section 3.5.

3.4.2 Switching frequency reduction

In many power electronic applications, limiting the number of commutations is a direct way of addressing the losses caused by switching frequency. In MPC, one of the many ways of controlling the switching frequency is to limit the change in the switching state. As would be shown in the results and can be derived logically, such a scheme would impact the quality of the current negatively but is sure to have greater control over frequency. Another method of reducing the frequency is to limit the variation in the voltage vectors selected, which gives an additional benefit of maintaining load voltage constant over a period. However, such a control would be inferior to the proposed solution due to its inability to directly counter the sudden increase in frequencies due to faults.

We began by assigning a vector for the switching states, wherein the elements are the active state of all the switches in the inverter as given by Equation 11.

$$S = (S_1, S_2, S_3 \ldots . S_N) \qquad (11)$$

Now, for the next instant, the state vector was represented by and so, the change produced when implementing the next step would be Equation 12.

$$n_f = \sum_{m=1}^{n} |S_m(k) - S_m(k-1)| \qquad (12)$$

Here S is the switching state, k is the current instant, and k-1 is the previous instant. Another method of implementing this logically would be the use of Exclusive OR logic in an iterative loop as follows:

```
for x = 1:6
   nf(i) = nf(i) + xor (states (x_old, k), states (i, k))
end
```

Including these factors, the cost function can be modified as Equation 13.

$$J = |i_\alpha^* - i_\alpha^P| + |i_\beta^* - i_\beta^P| + \lambda_c |v_{c1}^P - v_{c2}^P| + \lambda_f n_f \qquad (13)$$

Here again, λ_f represents the weight on the switching frequency reduction term.

3.5 Algorithm for the MPC

The MPC action can be summarised in the form of an algorithm as shown as a flowchart in *Figure 5*. Depending on the application chosen, the weights were tuned. In every time step, the load current was measured, back emf was determined and load currents corresponding to the next time step were predicted using the cost function by considering all possible cases and by choosing the vector with the least possible cost value. Depending upon the control objective, as shown in *Figure 5*, the cost function may include the weighting factors for capacitor voltage balancing and switching frequency reduction. Different power electronic applications require different control objectives and with MPC, it is possible to attend to these demands by assigning appropriate weights to the terms in the cost function. However, it should be noted that assigning equal or greater weights to secondary objectives resulted in a

decrease in the quality of the primary objective. Thus, control of additional parameters presented a trade-off in the quality of the primary objective and the effects were more profound with the increase in weights.

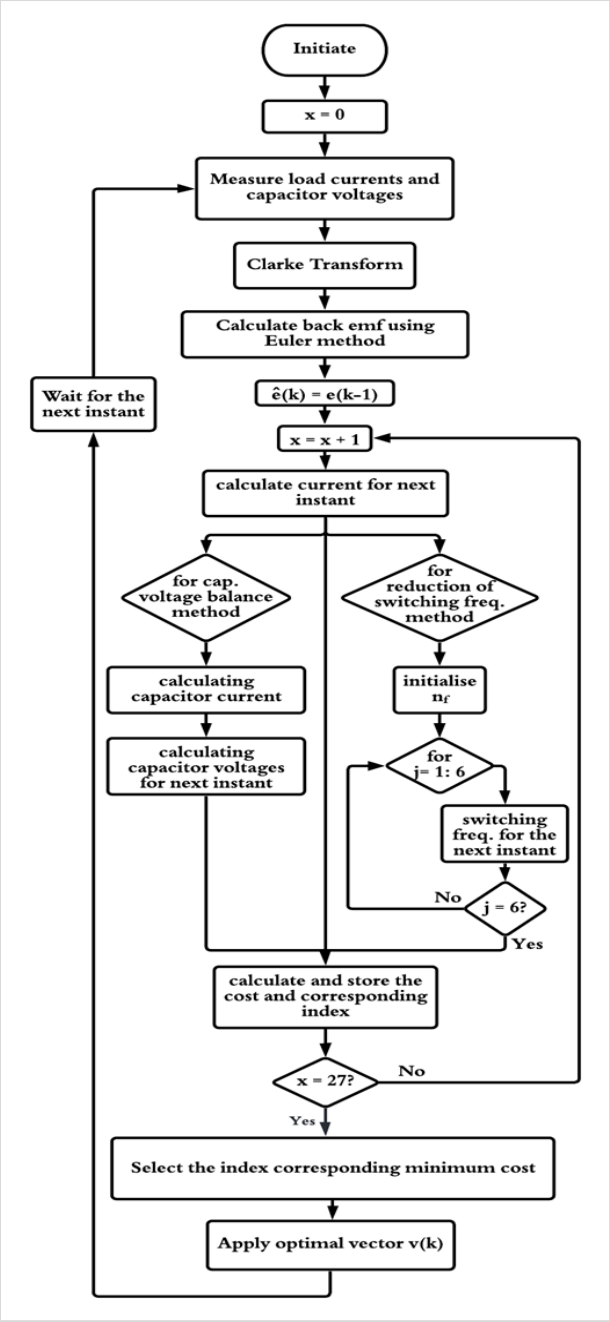


Figure 5 The algorithm represented in the form of a flowchart

In our case, in order to visualize the results of changing the weights, THD was chosen as the major testing parameter. The variation of THD with respect to weights in each case was evaluated. Furthermore, in order to understand the merits of MPC, the standard results were compared against those of a system controlled by PWM-PI linear control.

3.6 Implementation using FPGA

MPC for Single phase, single leg three-level inverter, 20VA, variable switching frequency was implemented as a prototype using Intel's DE0-Nano board. Hardware experimental setup was framed using four blocks, inverter-block, driver-block, load-block, and FPGA controller. The three levels of the inverter would need +30, 0, and -30 volts, which would be provided by a 60 volts source. As per the requirement, DC link capacitance was calculated as 1.33mF. IN4148 was chosen as the clamping diode to withstand high reverse voltage and surge current in case of fault and protect the inverter circuit.

MOSFET IRF540N was chosen with a driver IR2110 because it could be used for both the high side and low side and is most suitable for applications that work at high frequencies. The values of the resistance-inductance load were derived from the calculated value of impedance and are 27Ω and 11mH respectively. The load current was sensed by ACS712, a hall-effect-based linear current sensor. DE0-Nano board includes an 8-channel 12-bit A/D converter to connect with real-world sensors.

Various hardware modules were implemented on FPGA using a hardware descriptive language called, Verilog. It includes MPC to predict the current, serial peripheral interface (SPI) to transmit data synchronously, phase-locked loop (PLL) to match the frequency of the clock to the working frequency, and look up table (LUT) for generation of the sinusoidal wave which was given as a reference to the MPC. The overall block diagram created using the Quartus software for the implementation on the DE0-Nano board is shown in *Figure 6*.

3.6.1 MPC calculation using FPGA

The current prediction formula was implemented using Verilog by reformulating Equation 5 to Equation 14.

$$I_{pred} = \frac{((I_{meas} \text{ x } L) - (RT_S \text{ x } I_{meas})) + T_S(V(i))}{L} \qquad (14)$$

Here I_{pred} is the new current and I_{meas} is the measured value. R and L represent the connected load and sampling time is represented by T_s. Since the above formula involves multiple arithmetic operations, split up into multiple lines to ease the debugging and also to reduce the overflow errors. To

improve the accuracy, the division operation was kept for the last. It was then used in the cost function as per the concepts discussed before. Since logical operations were preferred for the implementation over the mathematical descriptions, switch operations based on cost function values were implemented by logical descriptive methods.

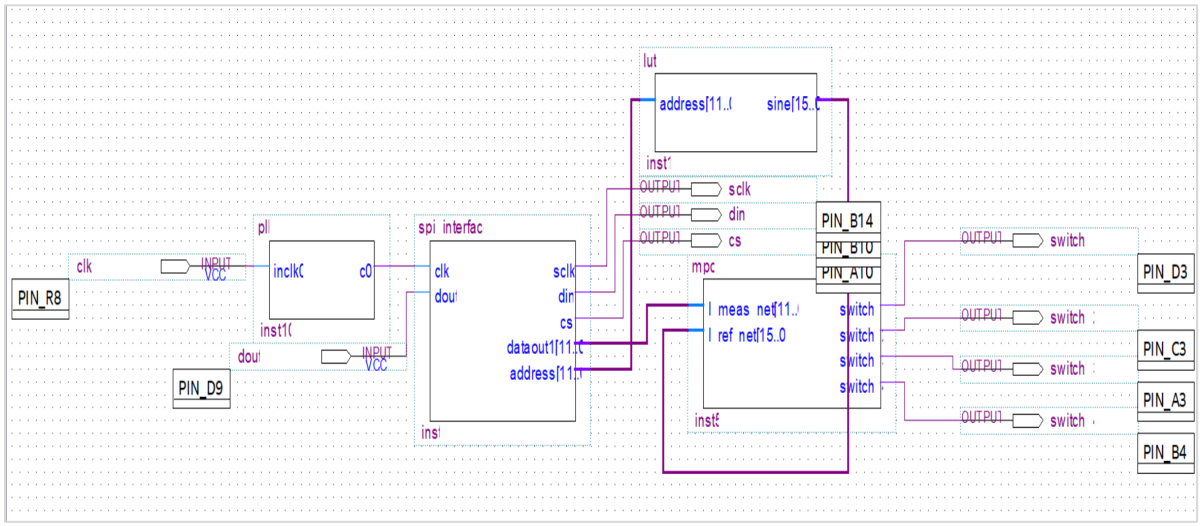


Figure 6 Overall block diagram on DE0-Nano Board, an FPGA platform, using Quartus

4.Results

Experimentation was performed using MATLAB/Simulink models and also using hardware setup of single phase, single leg three-level inverter with MPC implemented using Intel's DE0-Nano board, an FPGA platform. MATLAB/Simulink implementation of three phase three-level inverter with an MPC algorithm as a function block is shown in *Figure 7*. The values corresponding to each parameter for the experimentation are shown in *Table 2*.

Experimentations/Simulations were performed

1. To compare the THD of MPC with PWM-PI control for various inverters.
2. To compare the response of the system to dynamic changes and the extent of coupling between the control variables, in the case of inverter with MPC and PWM-PI control.
3. To analyze the effect of capacitor voltage balance weighing factor on the response
4. To analyze the effect of switching frequency weight factor on the response
5. To analyze the effect of controller sampling time on the response
6. To analyze the effect of inductive Load on power loss and power factor

4.1Comparison with conventional control

In the simulations, we compared the observations obtained from the PWM-PI control against the MPC control for a three-phase three-level inverter. In the PWM-PI control method, we used a PI controller where, by tuning the values of the controller gains KP and KI we could improve the response of the system, both steady state and dynamic to an extent. Tuning of the PI controller was done using Ziegler–Nichol's method. On the other hand, In MPC, the mathematical model for the control system was tuned by a heuristic method.

Usually, nonlinear systems are responsible for the improper performance of the PWM-PI control, which is not a fact for MPC control as it can handle both nonlinear and linear systems well, in turn showing better performance. There are 19 unique and eight similar output voltage space vectors for a three-level inverter, which each control system handles differently, causing the THD characteristics to be different. In *Figures 8* and *9*, the THD of load current for the three-level inverter with PWM-PI and MPC respectively are compared and observed that the THD of PWM-PI is more for the same parameters.

Table 2 System parameters for simulation

Parameters	Values
Input Voltage	400V
Load Resistor	100Ω
Load Inductor	0.1H
DC link Capacitor	4.7×10^{-5}F
Line Frequency	50Hz.

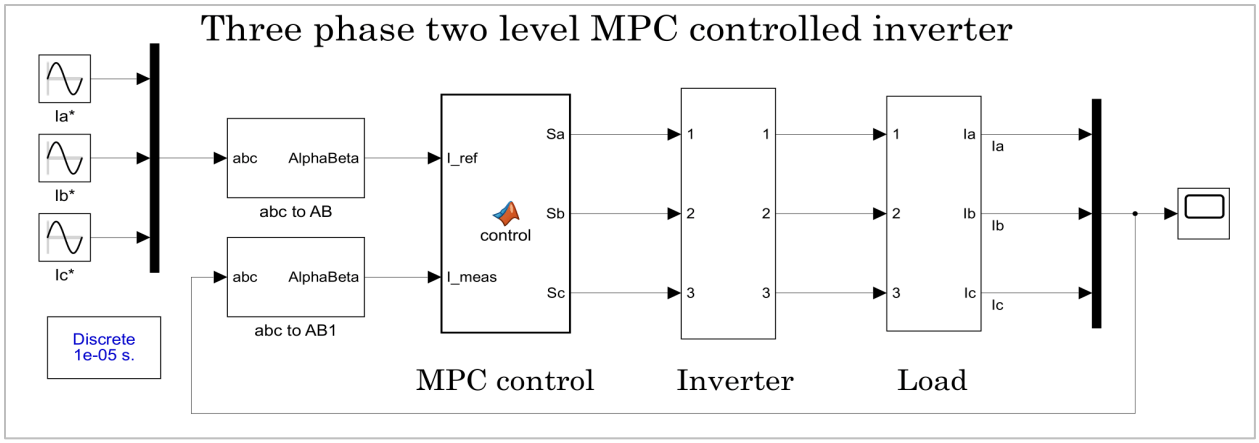


Figure 7 Block diagram for the MPC-based inverter implementation using MATLAB/Simulink

In PWM-PI control, harmonics were observed around the fundamental frequency (50Hz) and carrier frequency (1200 Hz) as the value of carrier frequency affects the lines of the system. In comparison, the THD of MPC was spread evenly throughout the spectrum. However, the margin of difference was significant when we analyzed both the control methods with other inverter models, like a 1-phase inverter and 3-phase 2-level inverter. The results are shown in *Table 3* that a 1-phase 2-level PWM-PI configuration performs better than MPC, but the performance of the former scales down as the model complexity increases. The performance of MPC for smaller and simpler systems was not up to mark because it has a high number of control parameters, increasing computational complexity. However, in higher-level inverters, the base computation in the control system remained the same with needed changes according to the levels. Hence, the control complexity did not increase and can handle higher-level model configurations well.

Table 3 Comparing the value of THD under different control schemes

Parameters	PWM-PI	MPC-Based
1-phase 2 level	0.82	0.91
1-phase 3 level	1.39	1.06
3-phase 3 level	0.80	0.59

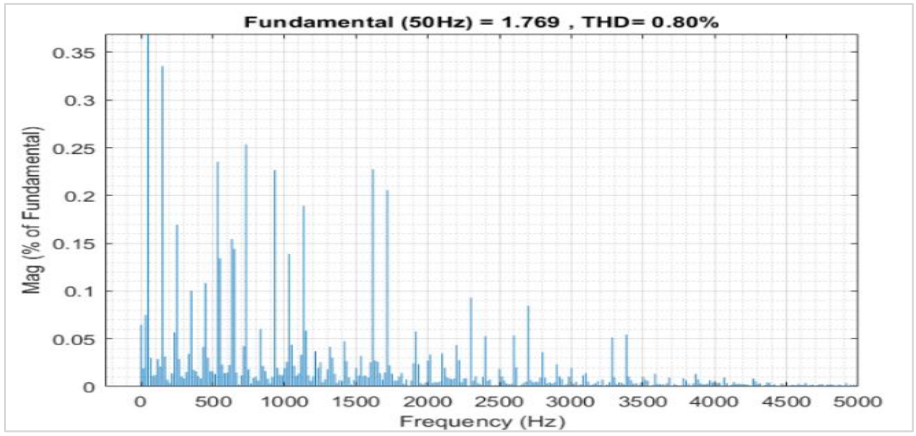


Figure 8 Fast fourier transform analysis of PWM-PI inverter

Subjecting the reference current to a step signal was useful in understanding the response of the system to dynamic changes and the extent of coupling between the control variables, here the load current. In this test, a step signal was introduced in one of the reference signals phases (here alpha phase) and the other phase was unaltered. Here, the reference current for the alpha phase is reduced from 1.6 Amps to 0.6 Amps at t=0.063 sec.

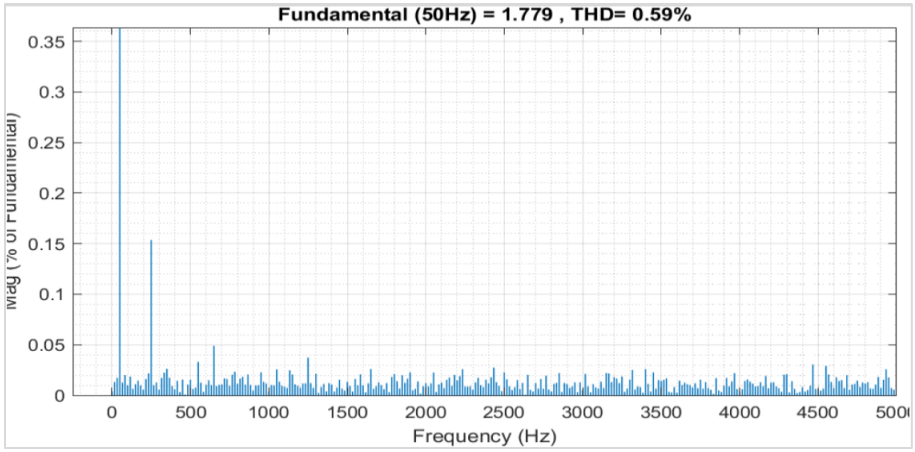


Figure 9 Fast Fourier transform analysis of MPC-based inverter

Figures 10 and *11*, shows the step response of the alpha signal and the corresponding change in beta signal for both PWM-PI control and MPC control respectively. The upper part of *Figures 10* and *11* clearly shows the reference tracking capabilities of these control techniques. However, in the case of PWM-PI control, a change in the beta signal can be observed with the change in the alpha signal. It showed that the coupling between the two reference phases was significant in the case of PWM-PI control, however, observed only a very negligible degree of coupling between the two phases in the case of MPC control variables. From this point forth, the simulations were conducted solely on the MPC system.

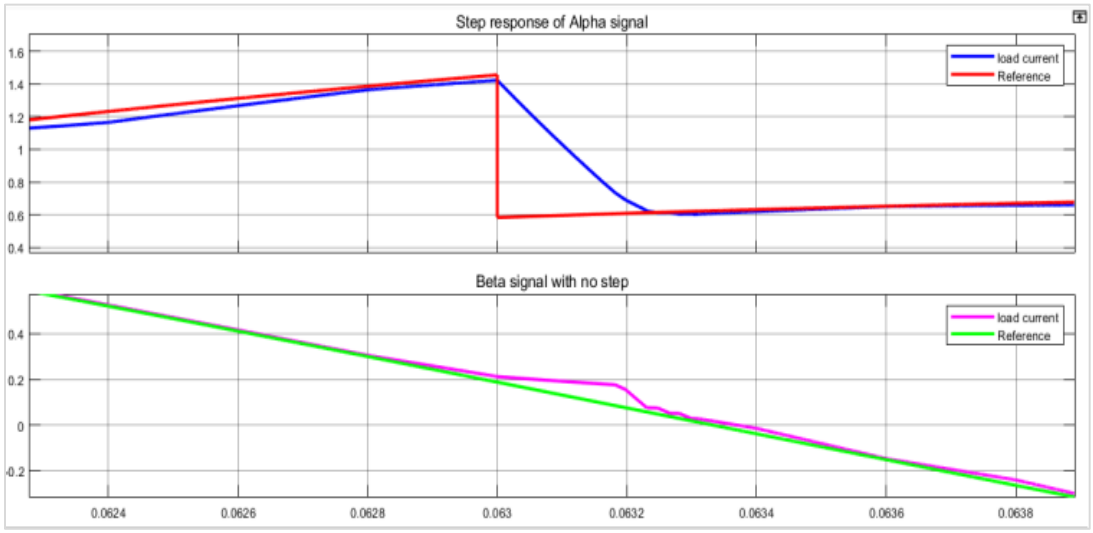


Figure 10 PWM-PI controlled system response

In our MPC-based inverter using the DE0-Nano board, it was observed that the predicted value of load current almost followed the measured value of load current which varied with the variation in gate signals of four switches. The results corresponding to the register-transfer level (RTL) simulation using the Quartus software and the output of the signal tap analyzer are demonstrated in *Figure 12(a)* and *(b)* respectively.

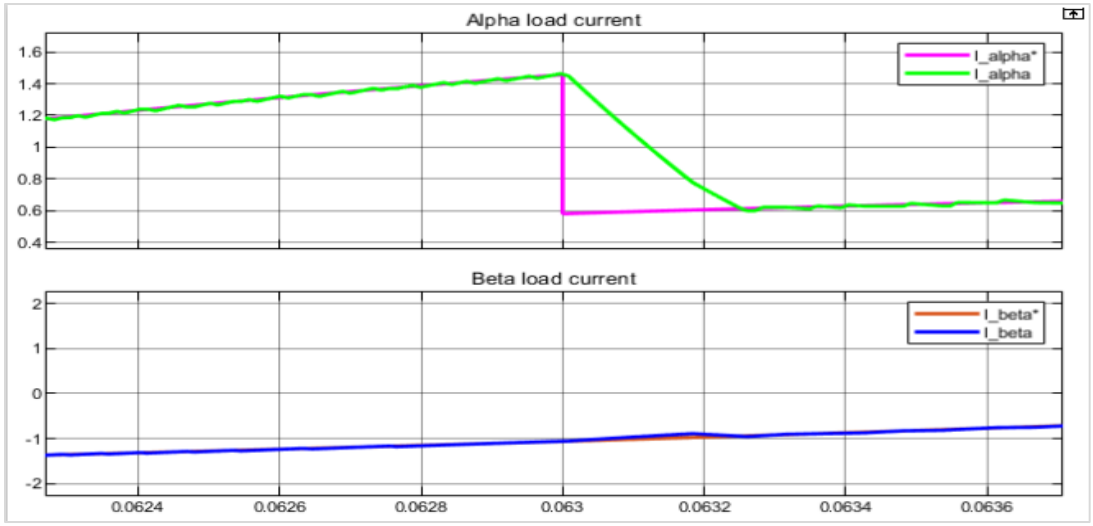
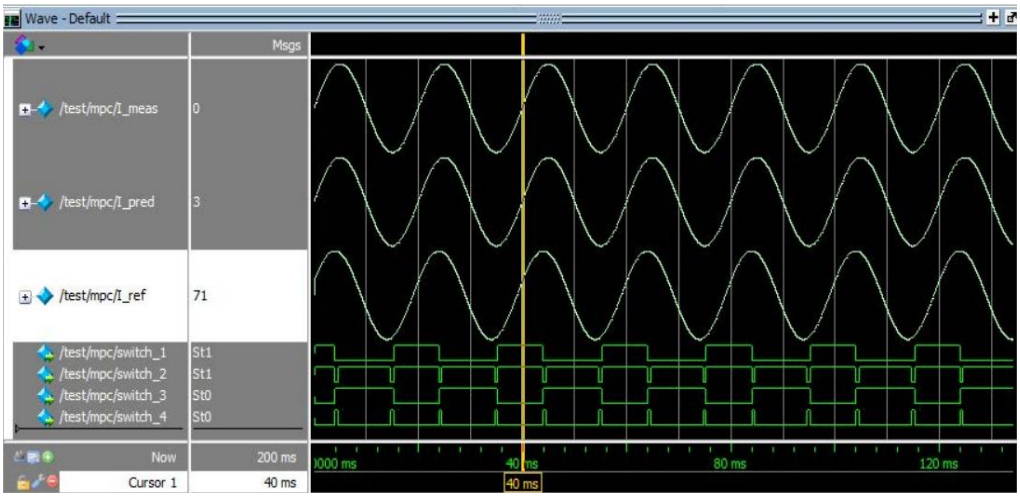
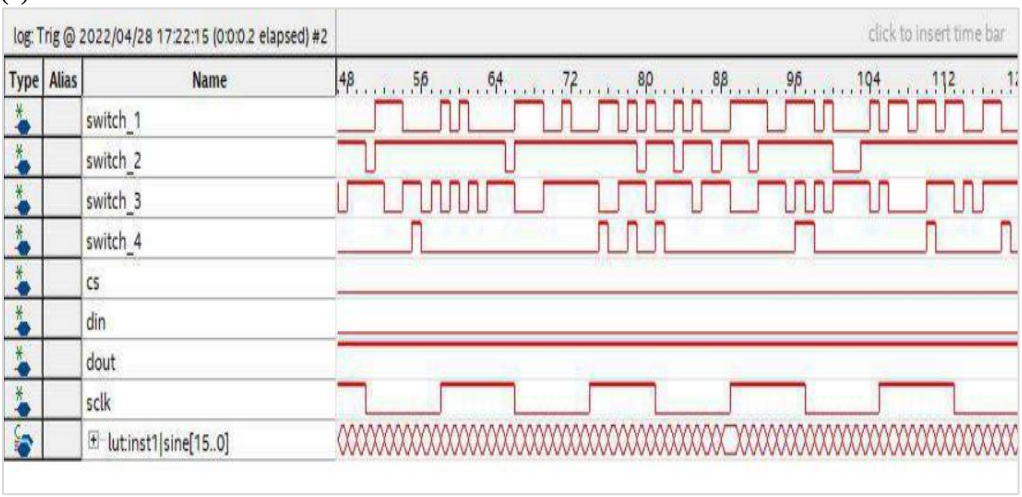


Figure 11 MPC controlled system response



(a) RTL Simulation



(b) Output from signal tap analyzer

Figure 12 Measured, predicted and reference currents and the gate signals for the switches

4.2Effect of weighing factor for capacitor-voltage-balancing

Balancing the capacitor voltages to their rated values was necessary for the safe operation of the inverter since, at an unbalanced state, both voltages across the capacitors quickly begin to separate, thus introducing considerable output voltage distortion, which may in turn damage the capacitors. As the weight gradually increases, the charging and discharging of capacitors may cause an increase in the switching frequency. With a high value of weighting factor, voltage unbalance was controlled to the extent that the controller now eliminates options of states that would lead to unbalance but at the expense of losses caused due to an increase in switching frequency. *Figure 13* shows the capacitor voltages for three different weight factors, λ_c=0, λ_c=10^{-5}, and λ_c=0.01. It clearly shows that the weighing factor λ_c=0.01 is the best for capacitor voltage balancing but, as mentioned, it may cause an increase in the switching frequency. Therefore, λ_c=10^{-5} was the recommended value for the weighting factor.

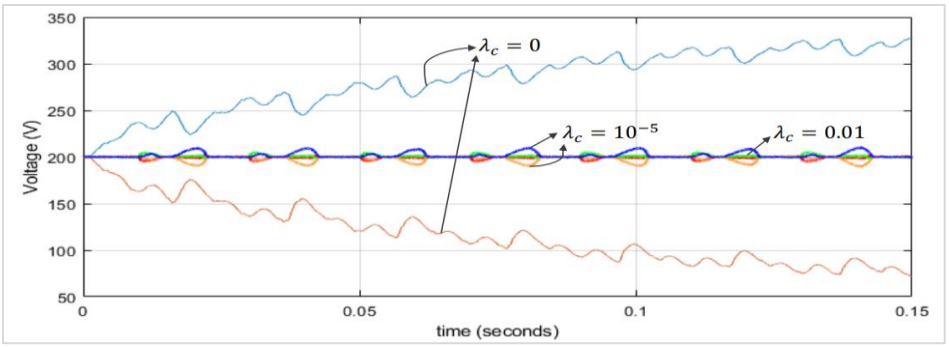


Figure 13 Capacitor voltages for different weight factors for capacitor voltage balancing

4.3Effect of weighing factor for switching frequency reduction on response

The results in *Figure 14* showcase the current and voltage waveforms at the inverter output across three scenarios of increasing weight on the switching frequency reduction terms of the cost function. Observation of the figure results in an understanding that for a more significant value of λ_f, higher distortion was seen in the load current because now the effort was to reduce the commutation of switches, which thereby compromises the controller's ability to match changes in the other variables. On the other hand, control over the output current worked best for λ_f=0 except that it had higher switching losses. Thus, an intermediate value of the weight was recommended for systems where the switching losses minimization was not a crucial objective as current control.

4.4Effect of controller sampling time on response

The sampling time of the controller is inversely proportional to the number of calculations performed per second. Thus, a greater sampling time indicates that the system refreshes the present switching state after a longer duration and hence, such a controller action is not refined.

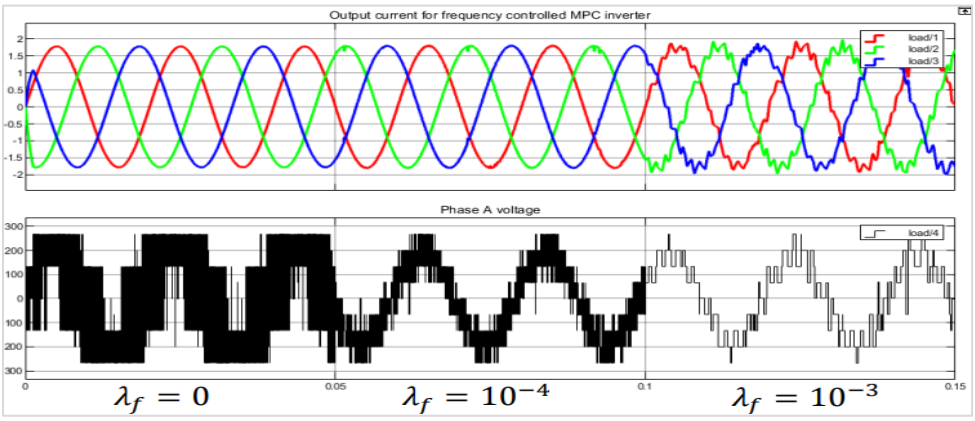
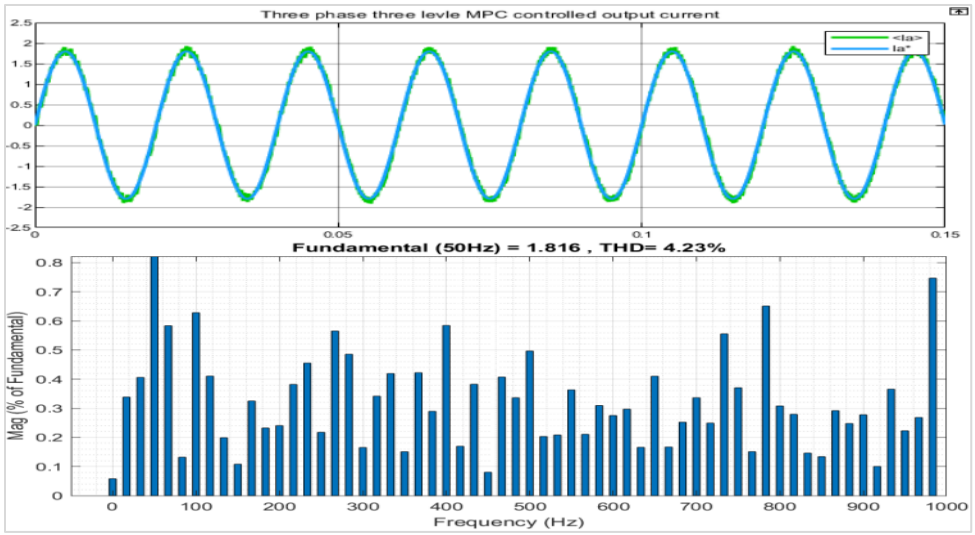
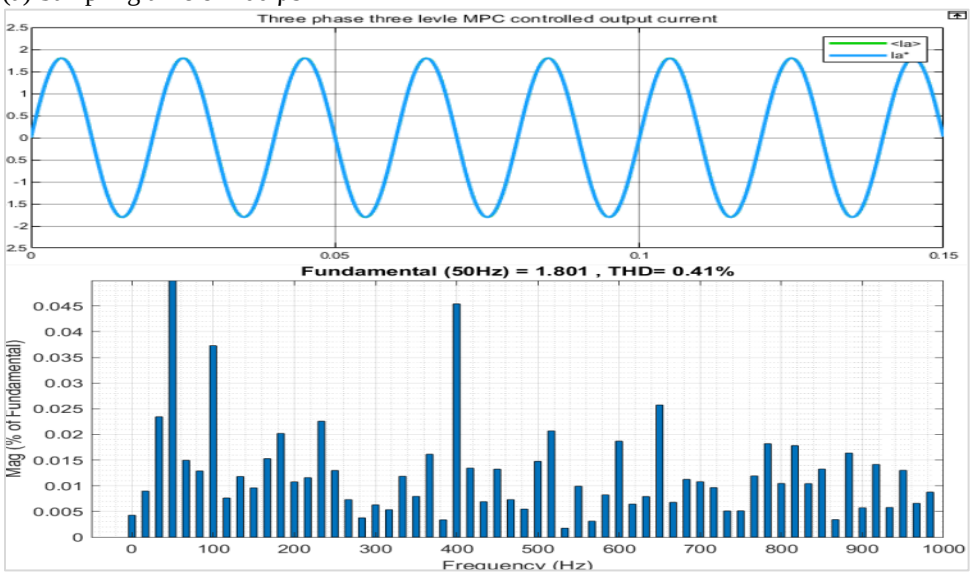


Figure 14 Effect of switching frequency weight factor on load voltage and load current

Figure 15(a) shows the output response of the system and the corresponding FFT with a sampling time of 100µs. Such a setting results in a slightly distorted waveform whose THD is 4.23%. Improving upon this action, the sampling time is reduced to 10µs in *Figure 15(b)* and the results improve to 0.41% THD and reduced distortion in the waveform. However, the smaller the sampling time, the greater the calculations per second, and thus, the computational stress on the controller was increased.



(a) Sampling time of 100 µs



(b) Sampling time of 10 µs

Figure 15 Load current and THD for different sampling time

4.5Effect of inductive load on power loss and power factor

Power loss under different power factors was also analyzed with simulations in the presence of the predictive controller and is shown in *Table 4.* As expected, it clearly indicates that the reduction in power factor leads to an increase in power loss.

Table 4 The inverse relation between power factor and power loss

Inductance (mH)	Power factor	Power loss (Watts)
0.1	0.986	9.42
0.3	0.831	116.82
0.5	0.423	400.22
0.7	0.208	548.62
0.9	0.106	618.87

5.Discussion

FFT Analysis of inverters with PWM-PI and MPC control shows that the load current THD is more in the case of MIs with PWM-PI control. It validates the difficulty of simple PWM-PI control to adapt to greater complexity in structure, which may lead to higher losses and distortion, resulting in higher harmonics.

The step response analysis (shown in *Figures 10* and *11*) shows that change in alpha reflects, change in beta also in the case of PWM-PI control. It indicates that the dynamics associated with the inner current control loop of PWM-PI control, result in significant coupling between the two reference phases. On the other hand, due to the capability of MPC to handle multiple parameters separately under the cost function, it is possible to see a very negligible degree of coupling between the two phases. Consequently, due to the aforementioned reason, the dynamic response of MPC is competitive with the PWM-PI control scheme.

The experimentation results based on the effect of capacitor voltage balance weighting factor on system response show that larger values result in less voltage unbalance. However, an increase in the value causes an increase in the switching frequency and thus more switching losses. Thus, in comparison, $\lambda c=10\text{-}5$ is selected as the best value. The results and discussions in subsection 4.3 lead to the conclusion that the weighting factor for the switching frequency reduction is not favorable to be a larger value because it affects the quality of the load current. However, as expected, the smaller value leads to more switching losses. Thus, the selection of a suitable value is very important.

Also, from the analysis of the impact of sampling time on load current, as per subsection 4.4, it can be observed that by reducing the sampling time, THD can be reduced. However, it may increase the computational complexity. Thus, the weighing factors and the sampling time need to be selected considering both the requirements and the computational complexity.

With an increase in inductive load, we saw a decrease in power factor which leads to an increase in power loss. This is due to the fact that active power dissipated at a load is independent of the power factor and depends solely on the voltage and current associated with the load. As cosine is a decreasing function, with an increasing value of phi (which is a result of increasing reactance), the power loss is increased.

Overall analysis indicated that the ease in considering non-linearities of the inputs with intuitive control design and complexity in the MPC-based control made it a viable option to switch for. In the case of single phase two-level inverters, PWM-based control had shown better results and the THD achieved was lesser in comparison with MPC. However, as we go up for more levels in inverters, the MPC-based control was a more reliable control method than the conventional PWM-based control.

5.1Limitation and the possible solution

MPC implementation for an inverter requires an accurate inverter model, cost function corresponding to various objectives, and possibly a larger prediction horizon for better performance. Because of these factors, the computational complexity of MPC is much larger as compared to conventional control techniques. By making the algorithms more parallel and by exploiting the parallelism using FPGA, the computational latency can be reduced. A complete list of abbreviations is shown in *Appendix I.*

6.Conclusion and future work

The paper presents an understanding of the merits of predictive control over conventional control methods for NPC topology by implementing a novel cost function that reduces distortions in current output along with the switching frequency reduction and capacitor voltage balancing. The scheme was effective in reference tracking and error elimination and showcases quicker dynamic response as compared to PWM-PI control. Moreover, due to its inherent nature, MPC presents a greater degree of decoupling between the control variables, which would be useful in applications handling signals from sensitive equipment. In addition to achieving primary control objectives, MPC can also be modeled to control other parameters of the system without the need of constructing inner loops. This not only helped with the dynamics of the system but provided the option to tune the control for these variables with minimum effort as shown in the results with capacitor voltage balancing and switching frequency reduction. DE0-Nano board, an FPGA platform was used for the prototype implementation to reduce the computational delay for the MPC.

It can be proven in the practical implementation of the two schemes mentioned in this paper, MPC would display a faster dynamic response as compared

to PWM as a consequence of dynamics of the inner loops in the latter delaying the response. The work presented in this paper serves as a skeleton to build upon and can be progressed further to control other topologies of multilevel converters. There is also a future scope of further refining the predictive control by introducing extended prediction horizons and including parameters such as switch dead time delays.

Acknowledgment
None.

Conflicts of interest
The authors have no conflicts of interest to declare.

Author's contribution statement
Akhilesh Mendon, Agnel Austin and Shraddha Ambilkar: Conceptualization, Investigation, Data curation, Writing – original draft, Writing – review and editing. **Shikha Menon**: Data collection, Conceptualization, Writing – original draft, Analysis and Interpretation of results. **Mini K Namboothiripad**: Study Conception, Design, Data collection, Supervision, Investigation on challenges and Draft manuscript preparation.

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Appendix I

S. N.	Abbreviations	Description
1	CCS	Continuous Control Set
2	DSP	Digital Signal Processor
3	FCS	Finite Control Set
4	FPGA	Field Programmable Gate Array
5	LUT	Look Up Table
6	MLI	Multilevel Inverters
7	MPC	Model Predictive Control
8	NPC	Neutral Point Clamped
9	PI	Proportional Integral
10	PLL	Phase-Locked Loop
11	PMSM	Permanent-Magnet Synchronous Motor
12	PWM	Pulse Width Modulation
13	RLE	Resistor-Inductor-Back-emf
14	RTL	Register-Transfer Level
15	SPI	Serial Peripheral Interface
16	THD	Total Harmonic Distortions