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Research Article

Design of silicon-on-insulator field-effect transistor using graphene channel to improve short channel effects over conventional devices

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Abstract
The conventional silicon channel metal oxide semiconductor field effect transistor (MOSFET) has fundamental limits that are reached due to scalability, resulting in short-channel effects (SCE) and other issues in small-channel devices. To overcome these challenges and design a nanoscale device, an alternate material was needed. Graphene, a novel material with exceptional properties, has been utilized to create a graphene field-effect transistor (GFET) optimized using silicon-on-insulator (SOI) technology. The SOI structure uses graphene as a channel, resulting in the development of a new silicon-on-insulator graphene field effect transistor (SIGFET) with an 18 nm channel length. The designed SIGFET exhibits significant improvements compared to traditional GFET and MOSFET. Specifically, the subthreshold slope (SS) of the SIGFET is 60.93 mV/decade, the drain-induced barrier lowering (DIBL) is 42.89 mV/V, and the ION/IOFF ratio is 6.55×108, which surpasses previous GFET-based contributions and SOI-MOSFET. Moreover, the effect of temperature change on SIGFET performance has been investigated, revealing that temperature variation only affects the drain current and has no impact on short channel characteristics. Therefore, the SIGFET can be an ideal substitute for traditional silicon channel devices.

Keywords
Graphene, FDSOI, Short channel effects, Low power FET, Graphene FET, Silvaco TCAD.

1.Introduction
The electronics industry is undergoing rapid growth with the rise of applications such as the internet of things (IoT), artificial intelligence (AI), and robotics. These applications rely heavily on hardware components like processors, which require nanometer-sized and power-efficient transistors [1]. However, conventional metal oxide semiconductor field effect transistors (MOSFETs) encounter fundamental limits at the nanoscale due to short channel effects (SCE) and performance degradation. Therefore, alternative nanoscale devices that offer low SCE and power-efficient properties are necessary to address this issue [2]. Designing nanoscale devices is not without its challenges. These include reducing leakage current, increasing ON current, maintaining parameter stability, improving reliability and yield, and lowering production costs.

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These challenges motivate the search for novel nanoscale devices that can overcome the limitations of existing technologies. The international roadmap for devices and systems (IRDS) [3] includes several alternative nanoscale devices that show promise in addressing these challenges. One such material is graphene, a highly promising two-dimensional substance with excellent electrical, thermal, and mobility properties. Graphene can be used to make the channel of a conventional MOSFET, thus improving its short-channel effects [4]. The graphene field-effect transistor (GFET), one of several new transistor structures in the nanoscale regime, has emerged as a potential alternative to the small channel MOSFET [5–7]. Due to the promising characteristics of graphene material, the GFET is one of the options for upcoming high-speed and low-power devices [8]. Another technological innovation that can be used to reduce power consumption in complementary metal-oxide semiconductor (CMOS) circuits is the fully depleted silicon-on-insulator

(FDSOI) technology. In this technology, a buried oxide layer is incorporated into the substrate below the channel of a device, which helps lower its off-state leakage current [9].

The purpose of this research is to develop a nanoscale field-effect transistor (FET) that can be utilized in low-power applications, with reduced SCE, by utilizing the unique and robust properties of graphene as a channel material. The study's main contribution is the application of FDSOI technology to enhance the short-channel parameters of the GFET. Another consideration for conducting this research is the improvement in key performance metrics, such as drain-induced barrier lowering (DIBL), subthreshold slope (SS), and I_{ON}/I_{OFF} ratio, which were achieved in a previous study [8] using Silvaco's technology computer-aided design (TCAD). The new device that was implemented and simulated in this study is called the silicon-on-insulator graphene field-effect transistor (SIGFET), which shows improvements in the DIBL, SS, and I_{ON}/I_{OFF} ratio. The current market for low-power nanosized transistors is being driven by a variety of applications, including portable devices, automotive electronics, networking infrastructure, biosensors, and household electronic appliances.

The paper is structured as follows: Section 2 presents a comprehensive literature review and identifies gaps in current research. Section 3 explains the design methodology for implementing the new structure, while Section 4 provides an in-depth analysis of the results. Section 5 discusses various characteristics and limitations. Finally, the paper concludes with Section 6.

2.Literature review

Jmai et al. [10] presented a tutorial on modeling and simulating GFETs using 2-D material electronics. The tutorial introduced graphene material, described various device structures, and discussed software simulation tools for circuit designs. Samal et al. [11] analyzed the performance of MOSFETs, comparing SOI and planar MOSFET technology. They observed that the SS increased while the leakage current decreased in SOI technology, making it suitable for low-power applications. However, they noted that SOI systems face challenges such as self-heating, the hot electron effect, and floating bodies. Aghaeipour and Naderi [12] reported a novel silicon-on-insulator (SOI) structure with two p+ pockets in the buried oxide at 30 nm. The reported drain current (Id) for this design is 1×10-4 A/µm, and the SS is 90 mV/dec. The design resulted in an improvement in SCE, reduction in temperature effects, and floating body effects. However, the critical fabrication process for creating additional pockets is a challenge. The reported DIBL for this design is 70 mV/V.

To enhance heating effects, Madadi et al. [13] developed SOI MOSFET at 32 nm. The impacts of floating bodies and leakage current both improved. The design's drawback is that various doping concentrations are required in various areas of the device. Reported SS=78 mV/V, Id(max)=0.1 mA/µm, and DIBL=142 mV/V. Mohammadi et al. [14] designed an SOI-MESFET having a gate length above 50 nm. Analytical modeling of the designed FET is carried out. Variation in work function is demonstrated. The reported SS is 70 mV/V, and the reported threshold voltage is 0.25 V. Anvarifard and Orouji [15] improved crucial electrical properties of a nanoscale SOI-MOSFET. Although the kink effect is diminished, the fabrication process still involves crucial steps because of the device's uneven structure. The reported DIBL is 40 mV/V, and Id(max) is 0.6 mA/µm.

Using FDSOI technology, Kwon et al. [16] created an n-channel negative capacitance FET. For a range of lengths between 30 nm and 50 m, the writers noticed an improvement in the SS and DIBL parameters. Reported DIBL = 47 mV/V and SS < 60 mV/V. Using FDSOI technology, Han et al. [17] created a phase transition FET. The device's OFF resistance is increased by utilizing multiple layers of material with a HfO_2/Al_2O_3 ratio of 3:1. The unusual design shows threshold voltage (V_{th}) = 2.12 V and Roff = 3.47 x 1011 Ω. The reported SS is 9 mV/dec, and the ION/IOFF ratio triples. A U-shaped channel of an FDSOI FET was simulated by Sudarsanan and Nayak [18] in a U-SOIFET. The novel structure differs from C-SOIFET in terms of body thickness, effective gate length, and gate area coverage. Observed that V_{th} and ION decreased as a result of this new structure. The variation in DIBL is also removed. Phase transition FDSOI MOSFETs without an external resistor for gate configuration have been implemented by Shin and Shin [19]. The channel length is set at 10 µm. The device shows SS=4 mV/dec. at Vgs = 0.96 V and reduces gate leakage current by 10 and 320 times, respectively, when Vgs = 0 V and 2 V.

A graphene tunneling FET was developed by Mazrouei et al. [20] utilizing methods that varied the band gap in the source and drain regions. With this

new structure, the device's I_{ON}/I_{OFF} ratio increases while the ambipolar conduction effect is reduced. This structure is suitable for digital switching applications. Using 2-D materials, Raju et al. [21] created a steep-slope transistor. utilized a layer of graphene in the gate stack. Up to 27.2 mV/dec. improvement in the SS was seen. Discovered a workable way to extend device scalability. Amor et al. [22] demonstrated the use of electro-thermal annealing to improve the performance of FDSOI. Up to a temperature of 590 K, an improvement in SS and Id can be seen. The stability of the device is also enhanced. A four-gate FDSOI was characterized at room temperature by Catapano et al. [23]. The four gates are seen to interfere with one another. To extract the device's performance at high gate voltages, a small model is developed. The model, however, is not examined for temperature change. The performance of FDSOI at cryogenic temperatures was examined by Xie et al. [24]. A highly doped backplane below buried oxide is used Improvements are shown in the V_{th}, transconductance, and drain current.

Yeh and Ohya [25] implemented an FDSOI-MOSFET employing a SiO_2-based low-temperature sputtering gate insulator. Improvements in mobility and SS values over thin-film transistors have been noted. Using an SOI substrate, Kwon et al. [26] developed a MOSFET for high-temperature applications. used the idea of carrier injection to cut down on temperature-related leakage current. At high temperatures, a material with a wide bandgap prevents carriers from entering the channel. A mathematical model was developed by Chatterjee et al. [27] to simulate FDSOI utilizing ferroelectric material. It calculates the impact of V_{th} on amplitude and pulse width. Compatible with exact industry-standard data reproduction. Two nanodevices were the subject of comparative analysis by Priya et al. [28]. To study SCE, an analytical model for V_{th} variation was created. To enhance device performance, backchannel inversion is a concept employed. It presents research on the SS, I_{ON}/I_{OFF} ratio, and V_{th}. Moreover, an implementation at the circuit level is done.

Double gate GFETs were reported by Chuan et al. [29] and the effect of scaling on device performance was examined. The non-equilibrium Green's function is employed in the Schrodinger equation. The SS and I_{ON}/I_{OFF} ratio are affected by the GNR width. The impact of temperature on the mobility of GFET was researched by Gosling et al. [30]. Studied the transit of charge carriers in monolayer graphene. It demonstrates thermal stability for various mobility values in single-layer GFETs. The benefits of employing multilayer hexagonal boron nitride (hBN) material as a substrate in GFET were shown by Fukamachi et al. [31]. The scalable fabrication process can increase the mobility of graphene material at ambient temperature. Encasing the graphene in another hBN material will increase its mobility. A graphene device was developed by Asad et al. [32] utilizing diamond as the substrate. The self-heating and material interference effects are intended. Reported fmax=54 GHz. The saturation velocity of graphene material is increased by diamond material. It works well with short-channel devices as well.

A new 2-D material FET technology was demonstrated by Estrada et al. [33]. Making a complementary inverter circuit involves combining 2-D materials. 90% noise margin and appropriate gain were attained. also improved the I_{ON}/I_{OFF} ratio and attained appropriate V_{th}. Using a graphene channel and boron nitride layer, Vali et al. [34] implemented gapless GFET. The interaction between the two materials results in an improvement in the bandgap. The I_{ON}/I_{OFF} ratio has significantly improved. The interlayer spacing affects the bandgap. By fabricating GFET, He et al. [35] solved the problem of edge roughness. The creation of a new graphene and carbon nanotube heterostructure for 5 nm technology is described. A technique for modifying nanotube unzipping time is created. It is possible to increase the GFET's mobility and ION/IOFF ratio. A two-gate graphene vertical tunnel field effect transistor (Gr-VTFET) has been published by Choudhuri and Bhowmick [36]. TCAD is used in a simulation approach that is demonstrated. The development in SS, DIBL, and I_{ON}/I_{OFF} ratio that was noticed. The gadget is appropriate for RF applications as well. Performance analysis of two distinct tunnel field-effect transistors (TFET) using graphene and phosphorene material was conducted by Shamloo and Goharrizi [37]. The parameters are obtained by solving the Schrodinger problem using the tight binding (TB) approach and the non-equilibrium green's function (NEGF) formulation. The I_{ON}/I_{OFF} ratio and SS in phosphorene TFET improved. The analysis of SS in cylindrical gate MOSFET was done by Jung [38]. The SS is impacted by changes in the doping profile. The SS is dependent on the straggle, and the value of SS is also influenced by the conduction path. The literature survey reveals that researchers employ various kinds

of FET structures. The short channel parameters DIBL, SS, and I_{ON}/I_{OFF} ratio must be optimized so the device can be used for low-power applications. Using Silvaco's TCAD, the SOI structure may be simulated below 20 nm and used to make the device perform at low power. SIGFETs can be designed using the traditional SOI-MOSFET configuration to improve performance. With minor improvements, the FDSOI technology can be employed in the cryogenic temperature range. The contact resistance of graphene material must also be considered.

3.Materials and method

3.1Block diagram of the design

Figure 1 illustrates a block diagram of the overall design. Initially, a literature review was conducted to determine the final device dimensions. Subsequently, FDSOI technology was utilized to implement the new structures. The Silvaco TCAD tool was employed to simulate a novel SIGFET structure, with appropriate meshing techniques employed. Additionally, an SOI MOSFET was simulated using the same dimensions for parameter comparison. The tool's numerical methods were utilized to extract various parameters from both devices. Various characteristics were plotted for both devices. A temperature fluctuation study was performed on the SIGFET to evaluate its performance at various temperatures. Finally, the performance of both devices was compared, and the results were contrasted with published data.

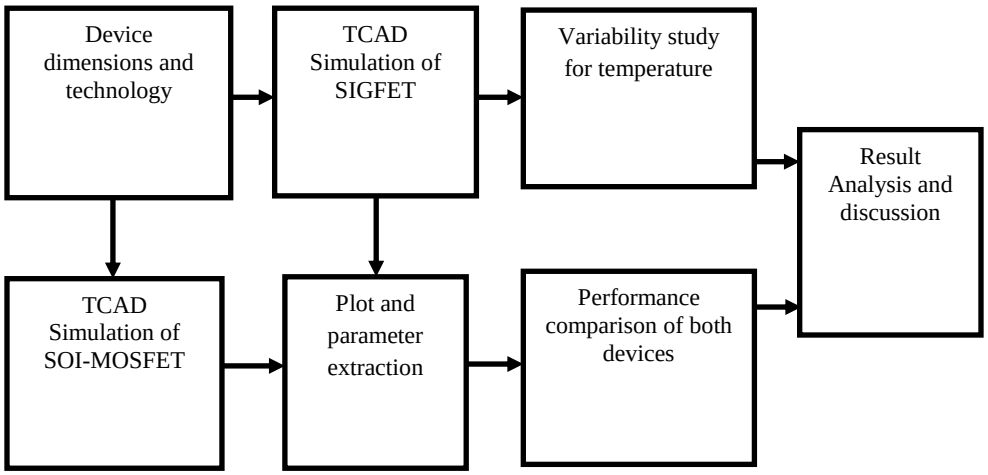

Figure 1 Block diagram of the complete design

3.2Silicon on insulator (SOI) technology

SOI technology is used to reduce the power consumption of a device. As in the conventional MOSFET device, the channel length is decreasing day by day. The device's ON current rises, but the OFF current, commonly known as leakage current, rises three times as well. This rise in leakage current raises a device's power need. A new method called SOI, which forms a thin layer of buried oxide (SiO_2) with a thickness less than the device's depletion width, is helpful in preventing this. As a result, it lowers the device's parasitic junction capacitor. This causes the device's I_{ON} current to increase, enabling high-speed operation. The SOI device also reduced the SS because it can operate on a lower V_{th}. The GFET of 20 nm channel length, which was designed in earlier work [8], is modified and SIGFET is designed to reduce the SCE further in this study.

3.3Structure of SIGFET

The SOI technology is used for further improvement of SCE for this design. A new device is implemented using Silvaco's TCAD [39], which has an SOI-like structure. The actual construction is seen in *Figure 2*. The device dimensions are selected by researching an 18 nm structure designed by Rawat and Paily [40].

The device has a 50 nm overall length from source to drain and a 40 nm depth from top to bottom. The source's contact length is 10 nm, while the source terminal is 16 nm long. The length of the channel region in the x-direction is 18 nm (it begins at 16 nm and finishes at 34 nm), and its depth in the y-direction is 4 nm.

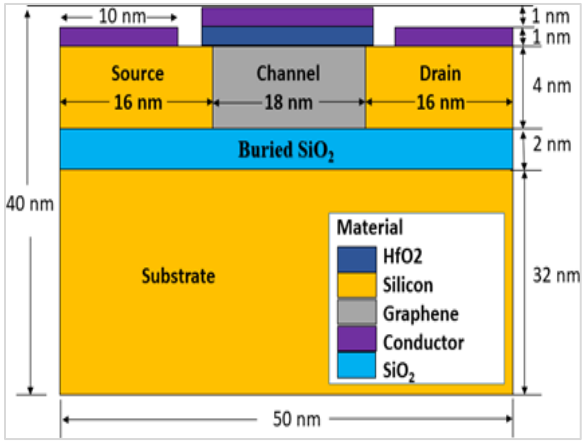

Figure 2 Structure of 18 nm SIGFET

The thickness of HfO_2 dielectric material is 1 nm. Between 15 and 35 nm, this dielectric material is placed as an overlay on the channel. To supply gate voltage, a contact of conducting material with a thickness of 1 nm is made. A SiO_2 insulating layer is created with a 2 nm thickness that varies between 6 and 8 nm in the y-direction. The depth of the substrate is 32 nm, with a range of 8 to 40 nm. The substrate has a potential of 0 V. Graphene material is not present in the TCAD tool's library, so in order to create a channel, a new material with properties akin to those of graphene is defined. The features of an already-existing material are modified to define this substance, which is then used as a user-defined graphene substance. An experimentally obtained optical constant is used to define this new material [41]. The newly implemented material is applied in line with the research from [8]. *Table 1* shows the geometry and process parameters of the device. The substrate is doped to a concentration of 1×10^{17} cm^{-3}, while the source and drain are doped to a concentration of 1×10^{18} cm^{-3}. For channel material, the electron and hole mobility is taken to be 30000 $Cm^2/V.s$.

Table 1 Geometry and process parameters

S. No.	Parameter	Value
1	Channel length	18 nm
2	Source and drain length	16 nm
3	Source, drain, and Channel height	4 nm
4	Buried SiO_2 thickness	2 nm
5	HfO_2 thickness	1 nm
6	Source and Gate contact length	10 nm
7	Gate length	20 nm
8	Source and drain doping	$1x10^{18}cm^{-3}$
9	Substrate doping	$1x10^{17}$ cm^{-3}
10	Electron and hole mobility	30000 $Cm^2/V.s$

3.4SOI-MOSFET with 18 nm channel length

The conventional silicon channel MOSFET is also transformed into SOI structure. The Silicon channel SOI-MOSFET is implemented using the same dimensions as in *Figure 2*. *Figure 3* depicts the silicon channel SOI-structural MOSFET's layout. As a channel, silicon is utilized. The channel length of this device is held constant at 18 nm for similarity. In order to create the SOI structure, a buried oxide is employed, with a depth of 2 nm.

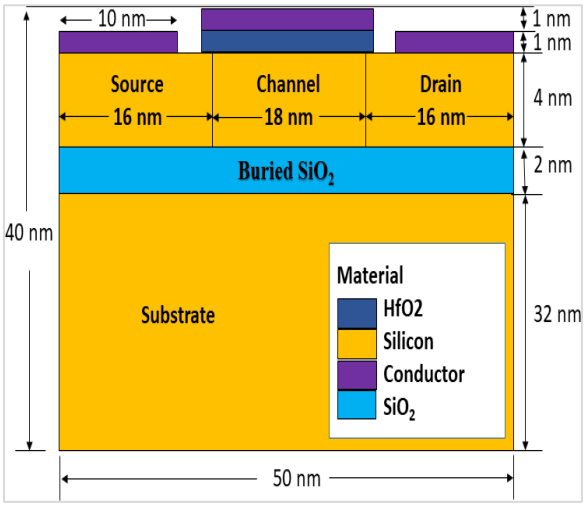

Figure 3 Structure of 18 nm Silicon channel SOI-MOSFET

3.5Models and numerical methods

A standard code sequence must be used in the Silvaco's TCAD tool to simulate a device. Numerical techniques and clearly defined models must be used for accurate simulations. For silicon materials at temperatures up to 300 K, concentration-dependent mobility (CONMOB) models are necessary. A fixed minority carrier lifetime shockley-read-hall (SRH) model is used to model minority carrier behavior. To simulate high current density conditions, the AUGUR model is employed. Strongly doped regions are modeled using bandgap narrowing (BGN). The velocity saturation effect is observed using a parallel electric field dependence model [39]. In the SOI structure, there is no electrode contact with the channel, and as a result, its potential is floating. This floating channel leads to a convergence problem when a potential is applied at the contact terminals. To solve this issue, the Gummel and Newton approach is used. This method employs Gummel iterations to enhance the initial predictions for Newton simulations, allowing for accurate simulation of the device.

4.Result

4.1Characteristics of SIGFET

Various characteristics of the implemented SIGFET are simulated and plotted. *Figure 4* illustrates the Id-Vgs curve, which shows that the device remains in the OFF state at low gate voltages, with a very low drain current. Once the gate voltage exceeds the threshold voltage (V_{th}), the device turns ON, and the drain current increases linearly with further increases in the gate voltage. The drain current reaches its maximum value when the drain-to-source voltage (Vds) reaches its maximum value of 0.8 V. The observed value of V_{th} is 0.22 V, resulting in a high I_{ON}/I_{OFF} ratio.

Figure 5 shows two curves for two distinct drain voltages, 0.8 V and 0.08 V, to illustrate the impact of DIBL. The gate voltage is varied for these fixed drain voltages, and the plots show the overlay characteristics. The measured value of DIBL is 25.95 mV/V.

In *Figure 6*, the characteristics of the drain current versus the Id-Vds are shown for three different gate voltages. The gate voltage for the first curve from the bottom is Vgs1=0.3 V, for the second curve it is Vgs2=0.6 V, and for the third curve, it is Vgs3=0.8 V, with Vds equal to 0.8 V. The device operates in both the linear and saturation regions. Initially, it operates in the linear region for a low drain-to-source voltage Vds, and then moves into the saturation region after a certain point. This behavior is like a traditional MOSFET. At Vgs1=0.3 V, the drain current is extremely low, at Vgs2 = 0.6 V, the device exhibits moderate current, and at Vgs3=0.8 V, the device exhibits sufficient current to switch.

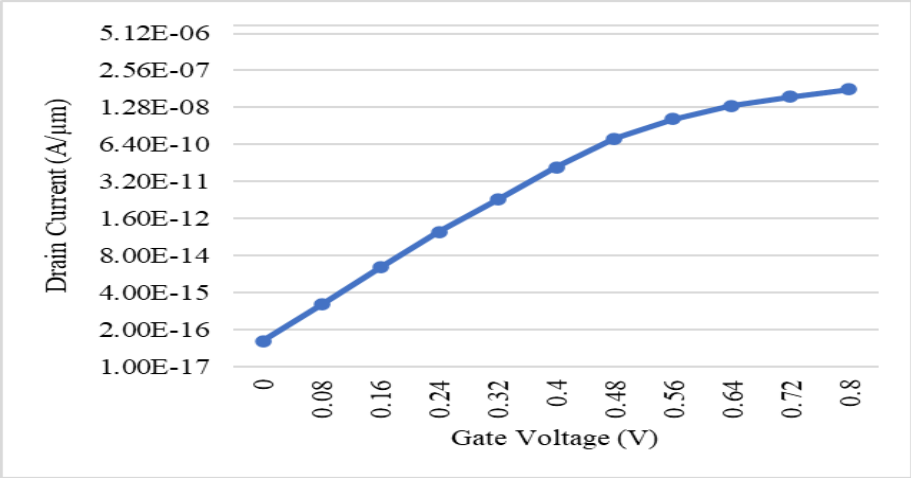

Figure 4 Id-Vgs Characteristics of SIGFET

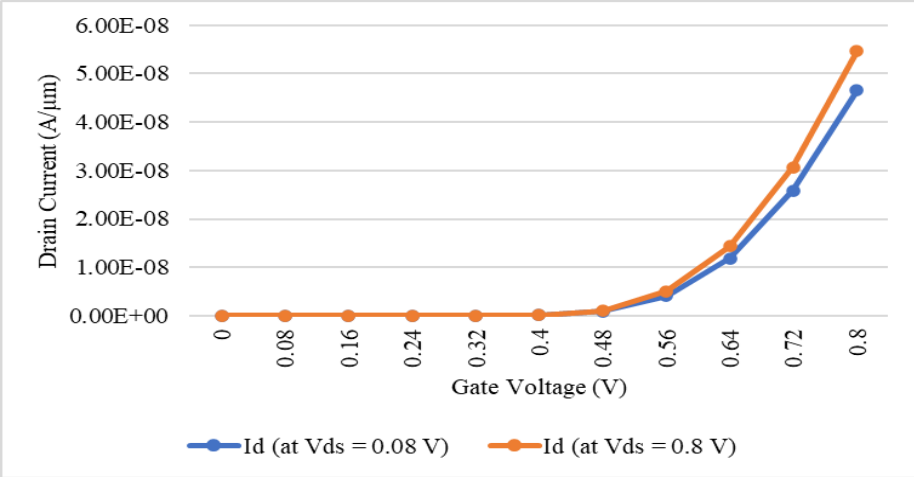

Figure 5 Id-Vgs Characteristics of SIGFET for DIBL calculation

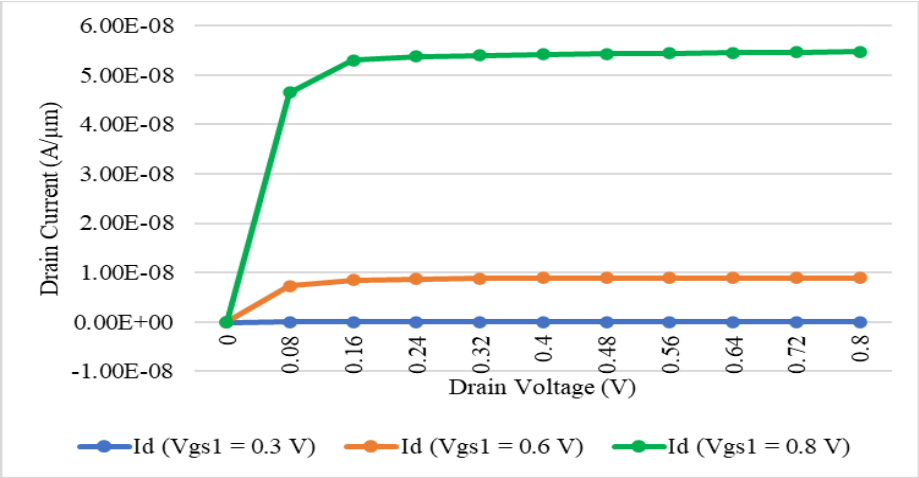

Figure 6 Id-Vgs Characteristics of SIGFET for three different Vgs

4.2Characteristics of SOI-MOSFET

The Id-Vgs curves of SIGFET and SOI-MOSFET are compared in *Figure 7*. The features show that they are identical; however, for Vds equal to 0.8 V, SOI-MOSFET produces a larger current. *Figure 8* depicts a comparison of the saturation curves of the two FETs. The drain current of SOI-MOSFETs is varied using three separate Vgs values. Vgs1 = 0.3 V in the first curve from the bottom, Vgs2=0.6 V in the second, and Vgs3=0.8 V in the third. This device has been seen to run linearly for low Vds values before entering a saturation area for higher Vds levels. The overlay properties are plotted to compare the effectiveness of the two devices. Vds is kept at 0.8 V as its maximum value. It has been observed that the implemented SIGFET has the same properties as the conventional device.

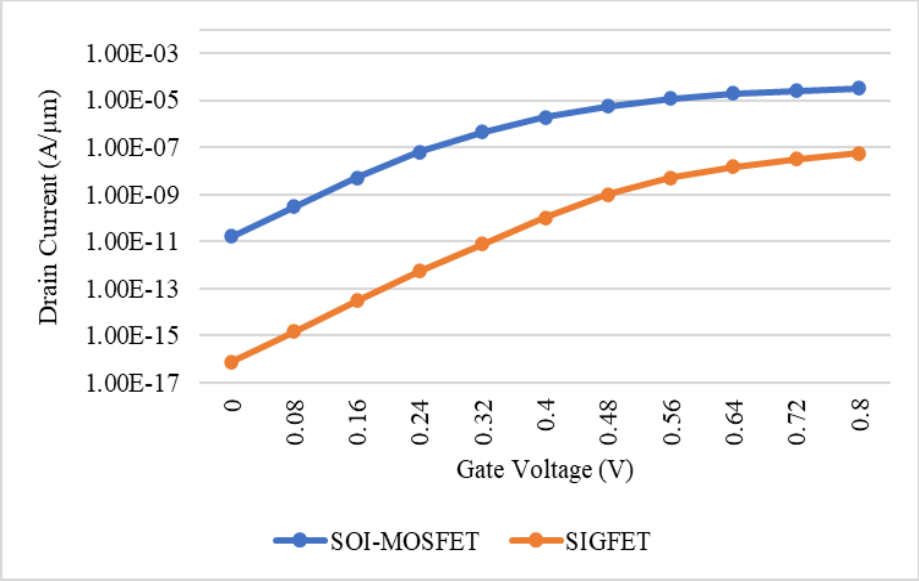

Figure 7 Comparison Id-Vgs curve of SOI-MOSFET and SIGFET

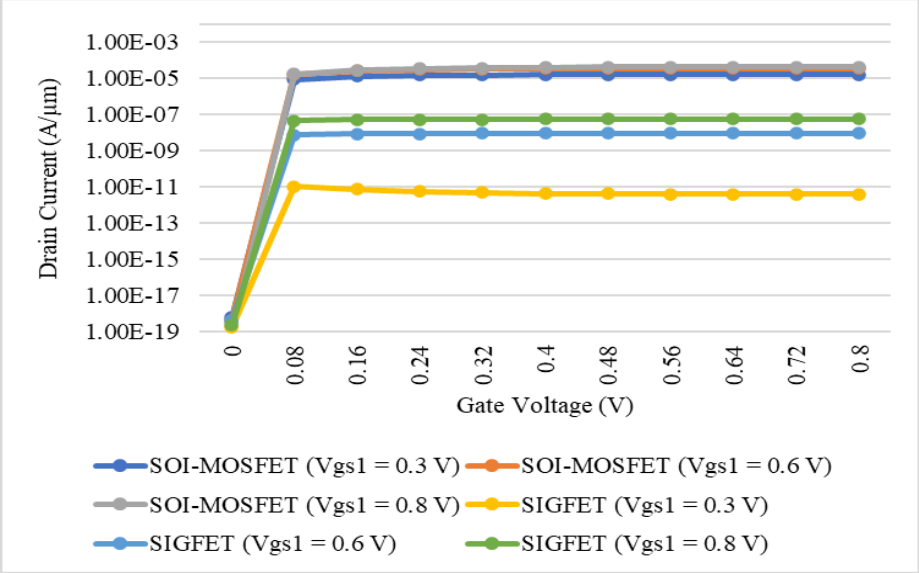

Figure 8 Id-Vds curve of both FETs

5.Discussion

The short channel parameters have improved as a result of the newly developed structure. A novel design that employs the SOI principle inhibits the leakage carriers, ultimately reducing the leakage current. The device's speed is increased due to the higher mobility of the graphene material. The obtained results show that the novel, promising material can be employed in the nanoscale regime alongside the SOI structure.

The SIGFET's newly implemented structure exhibits good compatibility with traditional MOSFETs. A GFET with a 20 nm channel was constructed in earlier work [8] using Silvaco's TCAD. The graphene substance was defined by the user. GFET was initially implemented at 100 nm, and then it was scaled down to 20 nm. The created GFET exhibits the same properties as traditional MOSFET. Although some SCEs have improved, there is still room for development in SCE for tiny geometry devices. This work implements a SIGFET with an 18 nm channel length. A comparison of the past and present efforts is shown in *Table 2*. When compared to the prior design and the SOI-MOSFET design, the I_{ON}/I_{OFF} ratio is seen to be equivalent to 698934853, which is extremely high.

5.1Result analysis

The SOI structure's buried oxide layer shields the channel from the potential which reduces leakage current and off current (I_{OFF}) and raises the I_{ON}/I_{OFF} ratio as a result. According to Equation 1, the I_{ON} is inversely proportional to the channel length L and directly proportional to the electron mobility (µn). The length of the implemented structure is also lowered to 18 nm, which also helps to improve the I_{ON}/I_{OFF} ratio. Graphene's mobility is also very high when compared to silicon material.

$$Id(lin) = \frac{\mu n.Cox}{2}.\frac{W}{L}.2[(Vgs - Vt)Vds - Vds^2 \quad (1)$$

SS is determined by Equation 2. The device's depletion capacitance (Cd) and the SS are inversely correlated. The depth of Cd is constrained by the SOI structure, which lowers the depletion capacitance. As a result, the SS value decreases, and the measured value of 61.03 mV/decade is close to the SS's optimum value. As HfO_2 is employed as a dielectric between the conductor and channel and has a larger dielectric constant than SiO_2 material, the value of Cox increases, the SS is inversely proportional to the internal capacitance generated by the oxide material, which is known as oxide capacitance (Cox). This rise in Cox value lowers SS as well.

$$SS = 60\left(1 + \frac{Cd}{Cox}\right) \quad (2)$$

Equation 3 is used to determine the DIBL. It depends on the V_{th} and supply voltage V_{dd}. The body voltage and permittivity of the substrate material are both factors that affect the V_{th}, which is inversely proportional to Cox. As the body becomes isolated in an SOI structure, the value of Vth changes, which changes the value of DIBL. Due to the buried oxide, the barrier that is created close to the drain terminal is not more affected. Hence overall it reduces the value

of the DIBL parameter. The value of DIBL has been observed as 25.95 mV/V.

$$DIBL = \frac{V_{TH}^{DD} - V_{TH}^{LOW}}{V_{DD}^{HIGH} - V_{DD}^{LOW}} \quad (3)$$

The observed value of V_{th} is 0.22 V, which is sufficient to turn the device ON and OFF while consuming minimal power. The observed drain current Id (max) is 0.055 mA/µm, which is close to the results of several implemented structures by various researchers that have already been published.

Table 2 Comparison of previous and present work

Parameter	SOI-MOSFET (This work)	SIGFET (This work)	GFET [8]	Fin-FET [42]	GNR-TFET [43]	SOI-MOSFET [12]	SOI-MOSFET [13]	GRDC-SOI [44]	Gr-VTFET [36]
Channel length(nm)	18	18	20	8	20	30	32	30	50
Vdd-max (V)	0.8	0.8	0.8	0.9	0.1	0.1	0.1	1	0.8
I_{ON}/I_{OFF} ratio	2001465	698934853	14379	10^6	116	--	--	10^6	$6.5x10^3$
Subvt (mV/decade)	63.99	61.03	114	63.13	27.4	90	78	60	8.53
DIBL (mV/V)	5.25	25.95	67.9	85	--	70	142	87	0.21
V_{th}(V)	0.04	0.22	0.040	--	--	--	--	--	0.18
Id(max) mA/µm	32.64	0.055	6.38	0.01	0.004	0.1	0.1	1.6	0.184

5.2Comparative study

The two designs used in this work are compared to the GFET designed in [8]. *Figure 9* shows the characteristics that contrasts the three devices' I_{ON}/I_{OFF} ratios. SIGFET has a higher I_{ON}/I_{OFF} ratio than GFET [8] and SOI-MOSFET implementation is around 698934853. The device uses less power when in a steady state because the leakage current is reduced. Comparing the properties of DIBL and SS is shown in *Figure 10.* The SIGFET indicates an improvement in SS that is close to the predicted value. The value of SS shows faster switching between the device's low and high states. To SIGFET, the DIBL is also lowered when compared to GFET at 20 nm. The V_{th} is enhanced by the reduced DIBL value.

Figure 11 compares the V_{th} and Id(max) of the three designs. When compared to the other two designs, it is shown that the V_{th} is higher in SIGFET. Due to the buried oxide layer employed in the device construction, the drain current Id (max) is shown to be reduced in SIGFETs.

The short-channel parameters of the SIGFET used in this study have been enhanced. The device was then subjected to temperature variation testing. As per reference [45], thermal effects cause changes in the channel temperature of FDSOI MOSFETs, which is due to the thickness and composition of the buried oxide, as well as the device's channel. At low temperatures, the device exhibits nonlinearity. Temperature changes were applied to the graphene-based device used in this study. *Figure 12* shows the characteristics of each parameter examined at various temperatures ranging from 100 Kelvin to 600 Kelvin. It can be observed from the temperature profile that the DIBL, SS, and V_{th} values remain relatively constant throughout the temperature range. The drain current Id stabilizes at a temperature of 300 Kelvin. However, even though the drain current is low at low temperatures, it still represents an improvement over [45].

5.3Limitations

Graphene material does not have a bandgap. To use it as a channel material in a FET, the bandgap of graphene must be expanded sufficiently. Other strategies can also be employed to open up the bandgap, such as the use of stacked graphene sheets or graphene nanoribbons with armchair edges. Since graphene is an extremely thin material, it is essential to fabricate FETs using conventional techniques. However, with the advancement of nanodevice fabrication techniques, this hurdle can be overcome. The constructed device exhibits low drain current values at lower temperature ranges, and additional work is needed to circumvent this limitation.

A complete list of abbreviations is shown in *Appendix I.*

Figure 9 Comparison characteristics of the I_{ON}/I_{OFF} ratio

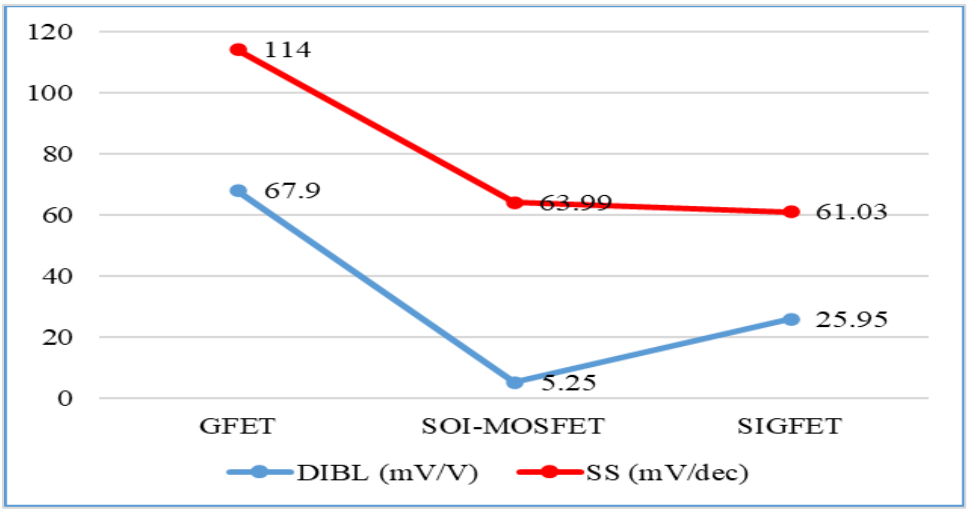

Figure 10 Comparison characteristics of DIBL and SS

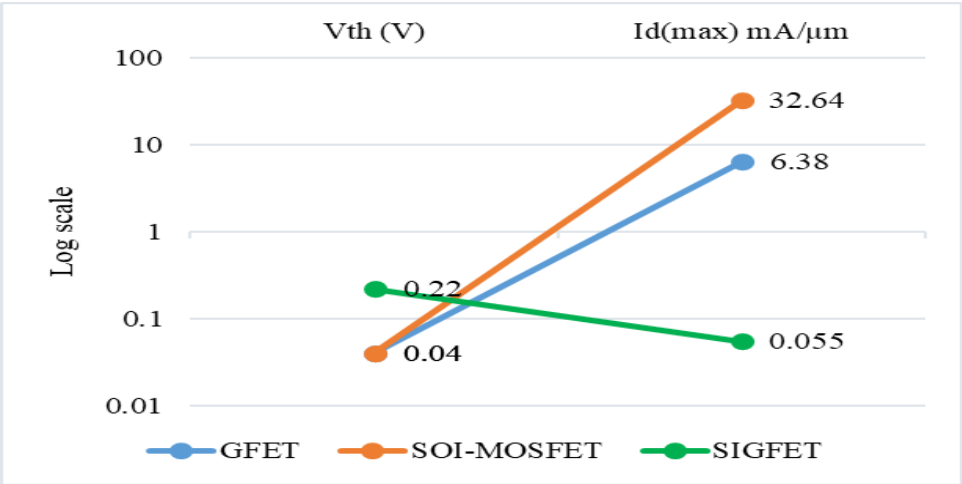

Figure 11 Comparison of V_{th} and Id(max)

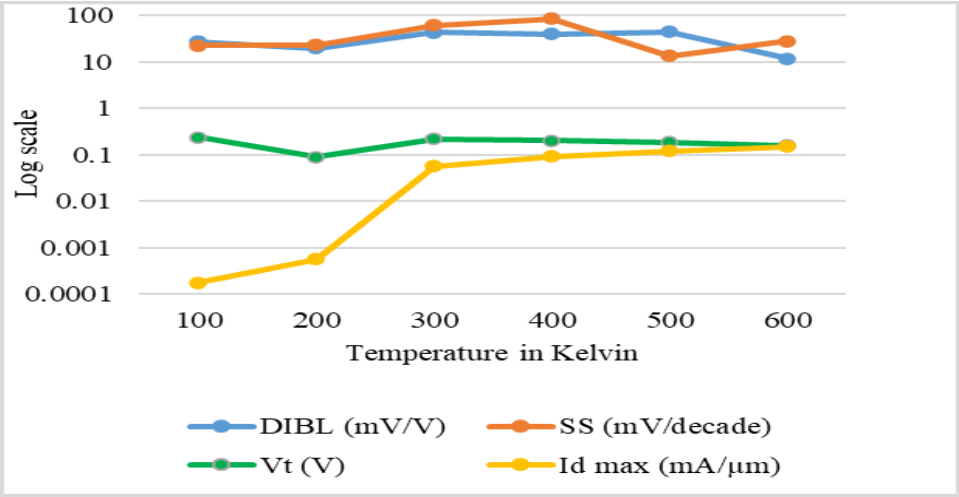

Figure 12 Temperature variation curve

6.Conclusion and future work

The SOI technology approach was utilized to fabricate a graphene channel FET. The device was modeled using SILVACO TCAD tool, and a Silicon channel SOI-MOSFET was used as a comparator device. The performance of the GFET created earlier at 20 nm was also compared to both FETs. Comparing the SIGFET to the other two designs and existing research, it shows improvements in terms of SS, DIBL, and I_{ON}/I_{OFF} ratio. The Id-Vgs and Id-Vds curves were plotted to compare the performance of these devices. Additionally, the temperature stability of the SIGFET was tested, and it exhibited exceptional stability. Thus, it can be concluded that this device can be used for low-power digital switching applications due to its high I_{ON}/I_{OFF} ratio and low SS value. Using a SIGFET in place of a classic SOI-MOSFET can lead to improved outcomes. Moreover, it will be possible to extract a simulation program with integrated circuit emphasis (SPICE) parameters for circuit development in the future using this device for low-power applications.

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None.

Conflicts of interest

The authors have no conflicts of interest to declare.

Author's contribution statement

Vinod Pralhad Tayade: Conceptualization, finalization of device dimensions, coding, result generation and interpretation and writing. **Swapnil Laxman Lahudkar:** Review, writing and editing

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Appendix I

S. No.	Abbreviation	Description
1	2-D	Two-Direction
2	AI	Artificial Intelligence
3	BGN	Bandgap Narrowing
4	Cd	Depletion Capacitance
5	CMOS	Complementary Metal-Oxide Semiconductor
6	CONMOB	Concentration-Dependent Mobility
7	Cox	Oxide Capacitance
8	DIBL	Drain-Induced Barrier Lowering
9	FDSOI	Fully Depleted Silicon On Insulator
10	FET	Field-Effect Transistor
11	GFET	Graphene Field Effect Transistor
12	GRDC-SOI	Graphene Retrograde Doping Channel Silicon-on-Insulator
13	Gr-VTFET	graphene vertical tunnel field effect transistor
14	hBN	hexagonal boron nitride
15	IoT	Internet of Things
16	IRDS	International Road Map for Devices and Systems
17	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
18	NEGF	Non-Equilibrium Green's Function
19	SCE	Short Channel Effects
20	SOI	Silicon-On-Insulator
21	SPICE	Simulation Program with Integrated Circuit Emphasis
22	SRH	Shockley-Read-Hall
23	SS	Subthreshold Slope
24	TB	Tight Binding
25	TCAD	Technology Computer-Aided Design
26	TFET	Tunnel Field-Effect Transistors
27	V_{th}	Threshold Voltage