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Research Article

Design a multilevel inverter circuit based on different control structures

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Abstract
Multilevel inverters (MIs) offer significant advantages over traditional inverters by generating higher output voltages with fewer distortions, making them suitable for high-power applications. In this study, a MI circuit was presented that had been designed and implemented with ten switches and four asymmetrical DC sources. It is controlled by two different techniques to achieve a 31-level inverter output. The controllers utilize a modified absolute sinusoidal pulse width modulation (MASPWM) technique and a phase disposition, level-shifted-PWM (PDLSPWM) technique. The arrangement of the four DC sources is set at (1:2:5:10) volts of direct current (Vdc). The system's performance is evaluated in both with zero level state (WZ) and without zero level (WoZ) state. Comparative analysis of the circuit during WZ and WoZ states, based on the PDLSPWM and MASPWM controller techniques, is conducted. Simulation results in MATLAB indicate that the total harmonic distortion (THD) values of the output voltage and current using the PDLSPWM technique are 0.6676% and 0.166627% during WZ state, and 0.8435% and 0.2625% during WoZ state, respectively. Conversely, using the MASPWM technique, THD values are 0.643% and 0.0757% at WZ, and 0.90158% and 0.10209% at WoZ state. These findings confirm the efficiency of both controllers in conjunction with the proposed power circuit, particularly noting that the MASPWM controller yields better results in the WZ state. Overall, the results demonstrate the effectiveness of the proposed MI circuit and controllers in achieving desired output levels with minimal THD.

Keywords
Multilevel inverter, Less switching devices, MASPWM, Phase disposition level shifted, Total harmonics distortion.

1.Introduction
Several power circuits and controllers using multilevel structures in electrical power systems have been discussed. With the people increasing in the world, the industries and electric power request have increased. Consequently, power systems become difficult and complex especially with non-linear loads [1]. Many industrial applications deal with medium and high-power devices. Therefore, multilevel inverters (MIs) are built to deal with the required power rating of these devices. Also, MIs can produce the required voltage and power with minimum output harmonics by increasing the output voltage levels. MIs can be supported by using renewable energy sources (RESs) [2]. The MI has some advantages than the two-level inverter type which involve a decreased dv/dt and increased efficiency [3–6]. The MI topologies are used to transform the direct current (DC) power to alternating current (AC) power and improve stability, efficiency, cost, and power quality of the system [7].

Power switches (SW) of MI are the main part that used to converter the input DC constant voltages to different AC voltage levels. They are determined the size of power circuit, connection reliability, control difficulty, and circuit cost. Reducing count of SWs compared to the conventional MIs reduces the size, cost, control complexity, and produce higher output voltage level [8, 9]. The main challenges of selecting MI's arrangement are developing the power circuits to get high power quality at the required voltage level with less SWs, complexity, and optimum control technique.

Different MI structures have been designed, but the cascaded H-bridge MI (CHMI) has gotten more attention. Based on the value of DC sources, the CHMI circuit is categorized into symmetrical MI (SMI) type and asymmetrical (AMI) type. To step-up the output voltage levels in traditional types (SMI), it is required to increase the number of H-bridges, which increases the SWs, gate drives, and protection circuits. In this case, the entire system is complex and costly.

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The main challenges for researchers are designing an inverter circuit and controller with flexible operation and minimum total harmonic distortion (THD) [10]. In the SMIs, the DC voltage sources have equal-value, while in AMI types, the DC voltages are unequal [11]. The AMI circuits apply fewer SWs, diodes, and DC-sources to get the same output levels compared with the SMI types [12]. To acquire higher output levels and less power electronics devices with high power quality, AMIs are designed to be a fundamental part in industrial applications such as RESs, high voltage DC systems, electric vehicles, etc. [13–16]. A few years ago, different topologies are suggested for CHMIs with different control methods [17–19]. Various topologies of SMIs are existing in [20–22]. The SMI topologies have benefits of low DC sources. While in the other side, many topologies need a large number of SWs, which is considered a drawback. A review of MI circuits with less SWs is done by [23, 24] and new topologies of MIs to reduce harmonics are implemented by [25, 26]. Also, many topologies of MI were considered based on less SWs [27–31]. Many studies discussed progress of MIs with less SWs such as the 'T' type MI, a new MI with less SWs, an improved switched diode MI, and a new diode-clamped MI structure with less SWs [32–35]. The use of less SWs in MI gets advantages such as minimizing cost, reducing power losses, and enhancing reliability that making these MI good for different applications, including RESs, motor drives, and power quality improvement [36]. This development of MIs with less SWs focused by researchers by improving the performance, cost, and complexity of these advanced power electronic devices. Increase number of levels produces smoothness in the MI's outputs [37, 38].

The difficulty in designing the MI is producing high output level with less SWs and high-power quality using controller circuit deals with any change occurs during operating the system. To outdo this challenge, a MI circuit is built with less SWs to produce different output voltage levels. Also, the proposed circuit and designed controllers built to track the required voltage level from 3-level to 31-level with distortion as minimum as possible, which is the main objective and contributions of this work.

The rest of the paper is organized as follows: Section 2 discusses the literature review. Section 3 covers the methods used. Results and their discussion are illustrated in Section 4. Finally, the paper concludes and summarizes in Section 5.

2.Literature Review

MI is widely used in high voltage and power applications because it produces higher number of levels that requires higher number of SWs, voltage stress, and DC voltage sources which making the system more complex and costly. To report this problem, numerous studies suggest new MI topologies with less SWs. In 2022, a new MI circuit with a hybrid control method introduced high voltage levels with a smaller number of SWs and low THD [39]. In 2023, a comparative study of many researches with less SWs of MI topologies were presented. Eswar and et al. are concerned with MIs as a converter with ON-grid based on RESs [40]. In 2023, authors provided a new MI with a low number of SWs compared with other topologies and discussed using a hybrid control method by combining nearest level and pulse width modulation (PWM) technique. Simulation and experimental results were presented and the results gave a low THD [41]. A new MI with a minimum number of SWs was designed to get a 25-level inverter fed by isolated unequal photovoltaics (PVs) as volts of direct current (Vdc) with (1:1:5:5) Vdc structure. a multi-carrier sinusoidal PWM technique was used. Simulation findings show that the THD values of single-phase MI's output voltage and current are 1.2% and 0.462%, respectively, while for three-phase MI's values are 1.07% and 0.342% [42]. A novel single-phase MI with 6 SW was designed to get symmetrical five-level and unsymmetrical seven-level inverter with sinusoidal pulse width modulation (SPWM) technique [43]. A MI using fewer SWs based on phase disposition PWM technique was designed to generates a low harmonic profile than other SMI and ASMI [44]. In 2016, a 13-level AMI circuit was constructed using 10 SW and 4 Vdc [45]. In 2020, a 9-level inverter was proposed and the THD of the output voltage was 13.5% [46]. In 2019, a novel switched DC source sub-module to create 13-level inverter with 10SW was built [47]. In 2019, a 15-level inverter based on 10SW and 25-level inverter using 12SW were implemented [48]. In 2021, a 15-level inverter with 3Vdc and 11SW was built [49]. In 2021, a 9-level with 11SW and 1Vdc with two capacitors as a voltage boosting capability was modelled and experimentally done [50]. In 2022, 3Vdc, 7SWs, and 3-diodes was used to create 15-level inverter [51]. In 2022, 81-level inverter circuit was built based on 16SW and 4Vdc [52]. In 2023, 11-level circuit with 8SW and 3Vdc was tested practically [53]. The above studies explain the challenges to produce a high-level voltage with fewer power electronics devices. In 2021, a 31-level inverter with 14SWs and four voltage sources of (1:2:4:8) Vdc arrangement was proposed [54]. References [55, 56] verified that the

output voltage gave approximately the same distortion value using phase disposition, level shifted, phase opposition disposition, and alternative phase opposition disposition PWM techniques with the CHMI. In 2022, a hybrid inverter based on half and full bridge circuit type using enhanced PWM technique was proposed to produce 11-level line-output voltage [57].

In this paper, based on past studies to acquire a comprehensive attentive of the MIs with minimum SWs and low harmonics distortion, a new arrangement of single-phase 31-level inverter is adopted and modelled based on phase disposition, level-shifted pulse width modulation (PDLSPWM) and modified absolute sinusoidal pulse width modulation (MASPWM) controller techniques with and without zero-level states as shown in *Figure 1*. The suggested topology is built to provide multi output voltage levels with minimum THD. The two controllers are programmed to drive the suggested circuit's switches. The innovative aspect of the proposed circuit is its ability to achieve a 31-level output voltage using a minimal number of SWs. The key contribution of this design is the enhancement of the power circuit's quality, which significantly improves the circuit's efficiency.

3.Methods

Suggested MI Topology

In the AMI, the power circuit is designed that the values of DC sources are unequal with different arrangement ratio and less SWs. In SMI circuits, the highest SW and Vdc to acquire M-level output voltages are calculated as shown in Equation 1 and 2:

No. of SW = 2(M – 1) (1)

No. of Vdc= (M – 1)/2 (2)

So, to have 31 output voltage level, the SMI circuit needs 60SW and 15Vdc. In the recommended circuit shown in *Figure 1*, the number of SW and Vdc are selected according to Equations 3 and 4:

No. of SW = (M–1)/3 (3)

No. of Vdc = (M – 3)/7 (4)

Consequently, number of SW and Vdc according to Equations (3) and (4) are ten SWs and four unequal DC sources. The number of SW and Vdc are reduced in this topology by 83.34% and 73.34%, respectively. The number of SWs and unequal DC sources are selected according to the circuit topology to produce 31-level output voltage. The 31-level output voltage switching patterns are clarified in *Table 1*. The structure arrangement of the DC sources is selected as (1:2:5:10) Vdc to get 31-level as number of levels will be created according this structure and current path explained in *Table 1*.

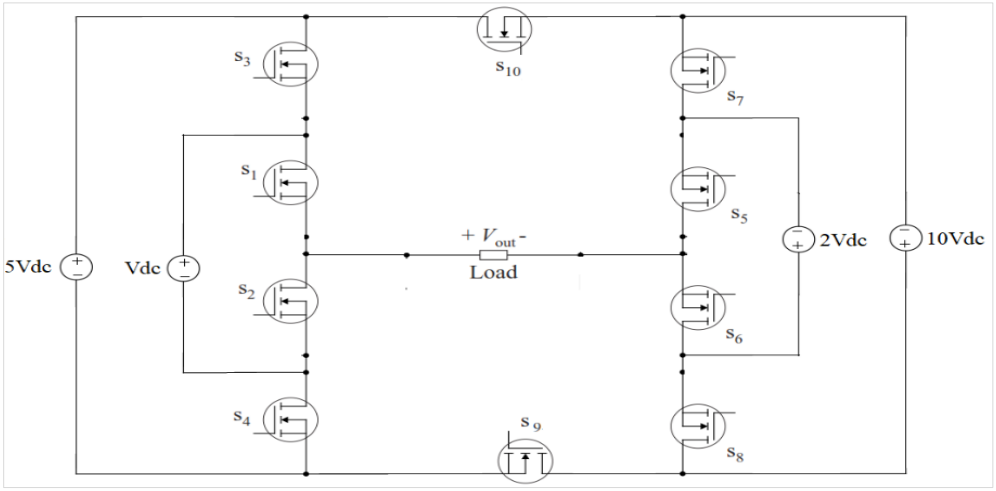


Figure 1 Suggested 31-level inverter circuit

Table 1 Switching patterns

Output Voltage	6Vdc	5Vdc	4Vdc	3Vdc	2Vdc	1Vdc
ON switches	2,3,5,8,9	2,3,6,8,9	2,3,6,8,9	1,4,5,8,9	2,4,5,8,9	1,4,6,8,9
Output Voltage	**12Vdc**	**11Vdc**	**10Vdc**	**9Vdc**	**8Vdc**	**7Vdc**
ON switches	2,3,6,7,9	1,4,5,7,9	2,4,5,7,9	1,4,6,7,9	2,4,6,7,9	1,3,5,8,9
Output Voltage	**-3Vdc**	**-2Vdc**	**-1Vdc**	**15Vdc**	**14Vdc**	**13Vdc**

ON switches	2,3,6,7,10	1,3,6,7,10	2,3,5,7,10	1,3,5,7,9	2,3,5,7,9	1,3,5,7,9
Output Voltage	**-9Vdc**	**-8Vdc**	**-7Vdc**	**-6Vdc**	**-5Vdc**	**-4Vdc**
ON switches	2,3,5,8,10	1,3,5,8,10	2,4,6,7,10	1,4,6,7,10	1,4,5,7,10	1,4,5,7,10
Output Voltage	**-15Vdc**	**-14Vdc**	**-13Vdc**	**-12Vdc**	**-11Vdc**	**-10Vdc**
ON switches	2,4,6,8,10	1,4,6,8,10	2,4,6,8,10	1,4,5,8,10	2,3,6,8,10	1,3,6,8,10

Controller algorithms

Switching configurations are very important for any MI to find the required output level. The harmonic distortion value is determined by the suitable control method based on PWM techniques. In this study, the control circuits using MASPWM and PDLSPWM controller techniques are adopted according to many studies that explained the effectiveness of the mentioned controller techniques. The PDLSPWM technique is built with carrier frequency of 3 kHz to get the required 31-level. The details of the PDLSPWM technique are illustrated in *Figure 2*. The modulation index is varied according to the required voltage level and carrier signal. The MASPWM technique is designed according to [2, 49, 51, 52, 58] to acquire the output voltage. The study is done with two cases. That means the controllers have ability to produce output voltage with zero level state (WZ) and without zero level (WoZ). So that, a comparison between these two controllers at these two cases are done to see which one is the best with minimum THD and low complexity. The two controllers are designed according to *Table 1*.

4.Results and discussion

To certify the importance of the projected MI circuit capabilities, simulation results by MATLAB program are discussed with input DC voltage sources of 12V, 24V, 60V, and 120V. Also, an inductive load (RL-load) of 70Ω and 200mH are examined through cases of WZ and WoZ states. The output voltage and current with its FFT spectrum of the recommended 31-level inverter using PDLSPWM and MASPWM techniques during WZ case at resistive load (R-load) and RL-load are shown in *Figures 3* and *4*, respectively. While *Figures 5* and *6* show the same waveforms during WoZ case. The THD values of the output voltage and current with RL-load during WZ and WoZ cases using PDLSPWMW technique are 0.6676%, 0.166627%, and 0.8435%, 0.2625%, respectively. While using MASPWM technique, the THD values at WZ and WoZ cases are 0.643%, 0.0757% and 0.90158%, 0.10209%, respectively. These results prove that the two controllers with the suggested power circuit are efficient and have good results. To check the power quality of *Figures 3-6*, the THD waveforms for the output voltage and current WZ and WoZ cases with RL load at different output levels are illustrated in *Figures 7* and *8*. Comparisons were made using the PDLSPWM technique during WZ and WoZ cases to determine which case yields better results. As depicted in *Figures 7* and *8*, the PDLSPWM-based WZ case produces superior outcomes compared to the WoZ case at various voltage levels. Similarly, comparisons with the MASPWM technique showed that the WZ case outperformed the WoZ case across different levels. Subsequently, the PDLSPWM and MASPWM techniques, specifically in the WZ case, were compared to ascertain the superior method. The results, as detailed in *Figure 9*, indicate that the MASPWM technique is more effective than the PDLSPWM WZ case. The 31-level inverter circuit using PDLSPWM and MASWPM techniques based on WZ case is compared with other related latest topologies based on number of SW, number of diodes (ND), total number of power electronics devices (NPE), number of voltage sources (NDC), structure of DC voltages (SDC), and THD of the output voltage (THDV) and current (THDI) as explained in *Table 2*. From the data in comparison *Table 2*, it is evident that the suggested circuit with the two controllers performs better than others, demonstrating the effectiveness of the designed system and controllers. The system is programmed with appropriate controllers that provide outputs under various conditions, ensuring good flexibility in response to any changes.

The highlighted of the designed MI circuit and controllers used in this study utilized less or same number of SWs and sources compared to other, but the power quality distortion is better than others. Good results are achieved using the suggested controllers. The circuit was modeled by MATLAB program and the results prove the effectiveness of the designed power circuit and controllers. The limitation of this study is the absence of laboratory facilities to implement the project practically.

A complete list of abbreviations is listed in *Appendix I*.

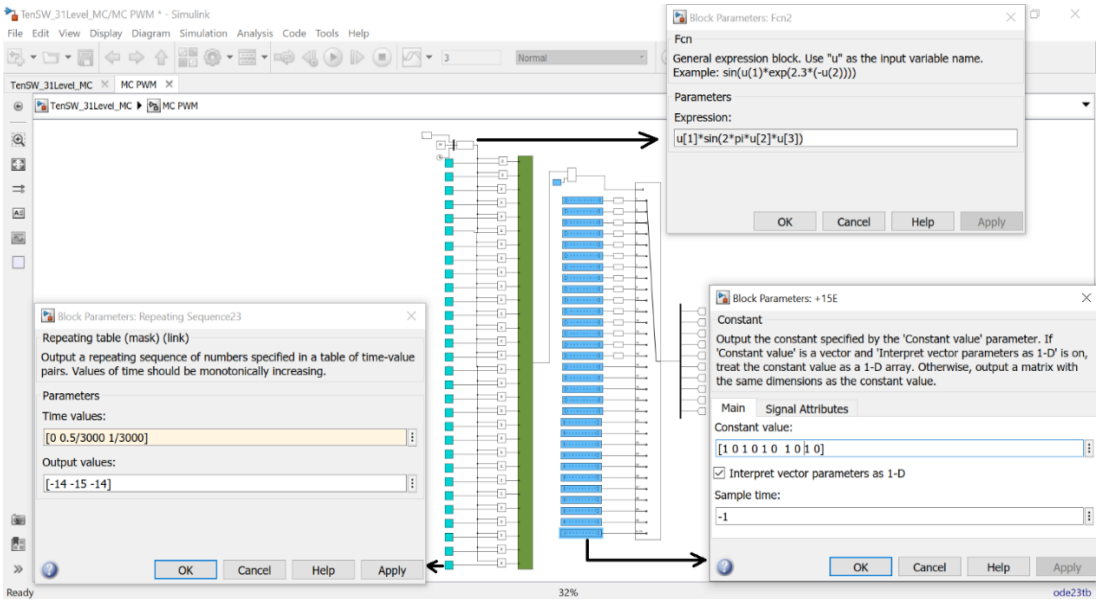
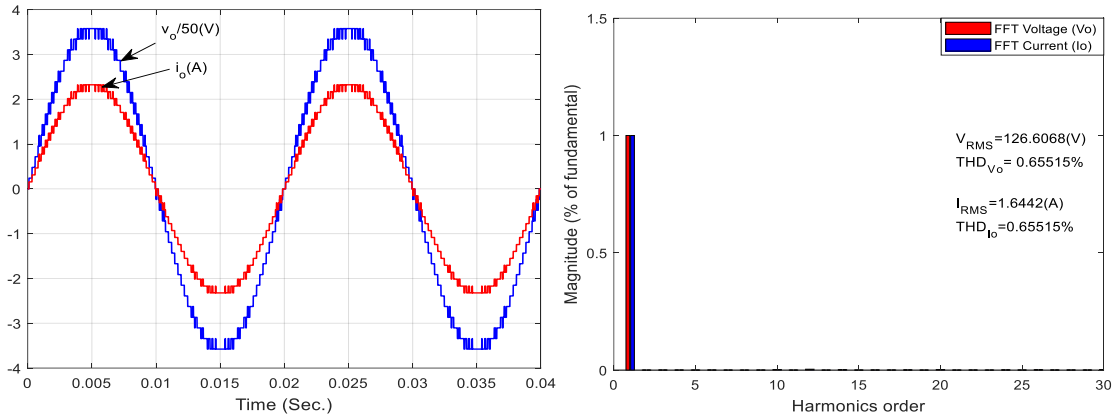
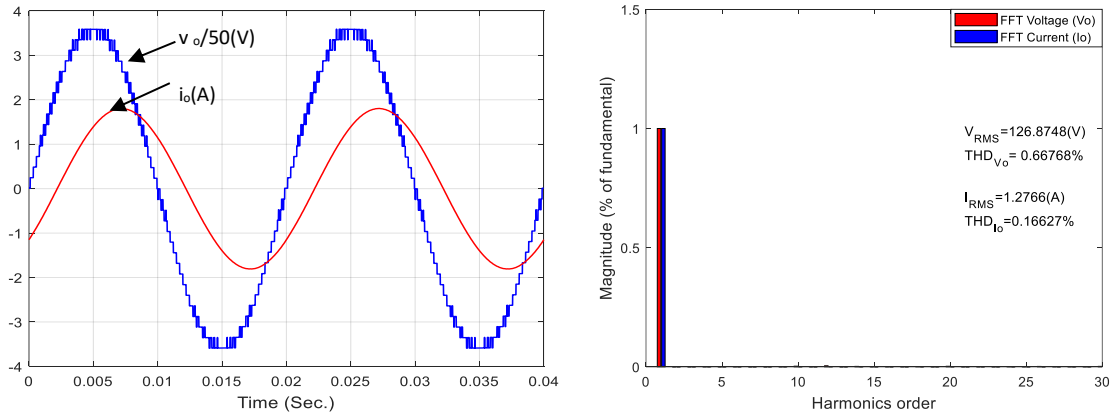


Figure 2 Modelling circuit of the PDLSPWM controller technique

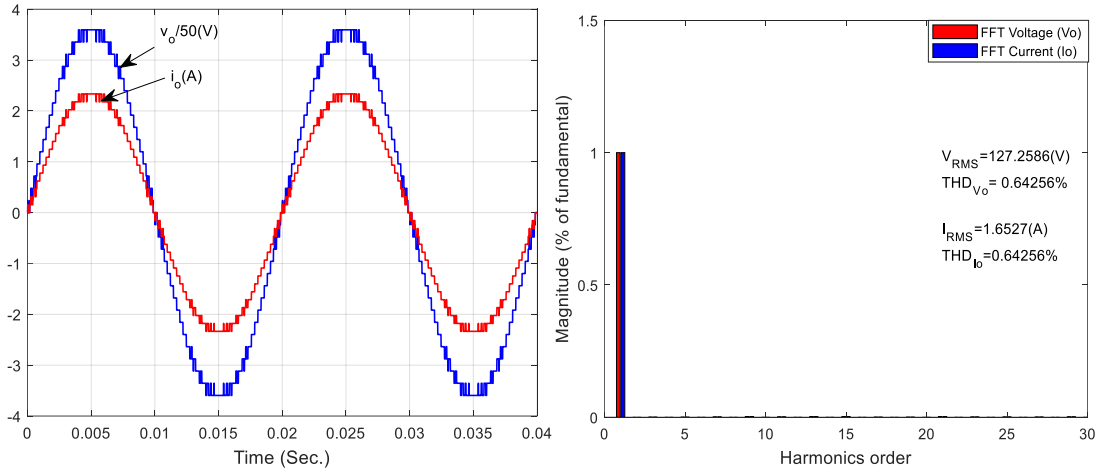


(a) R-Load

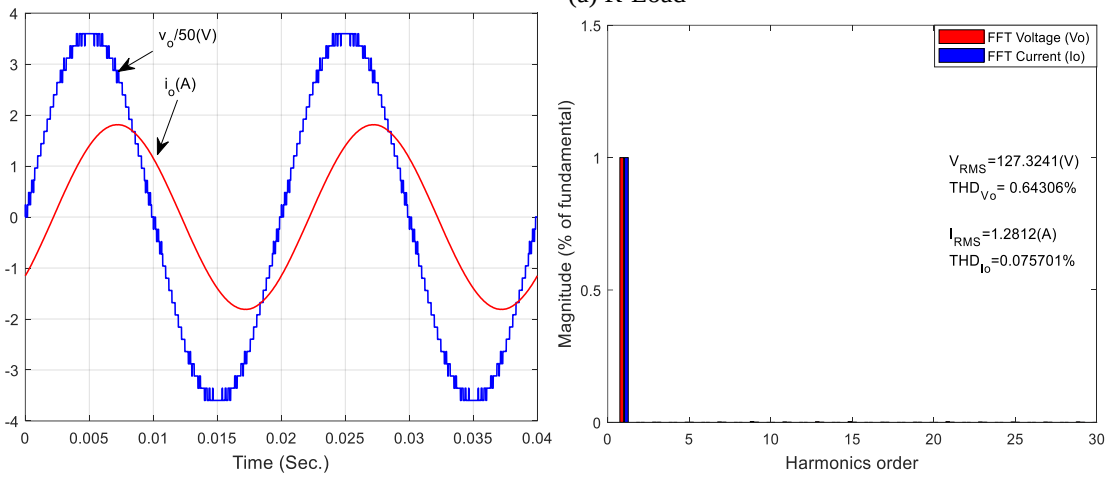


(b) RL-Load

Figure 3 Model outcomes of the 31-level output voltage and current and its FFT analysis based on PDLSPWM technique and WZ state (a) R-Load (b) RL-Load

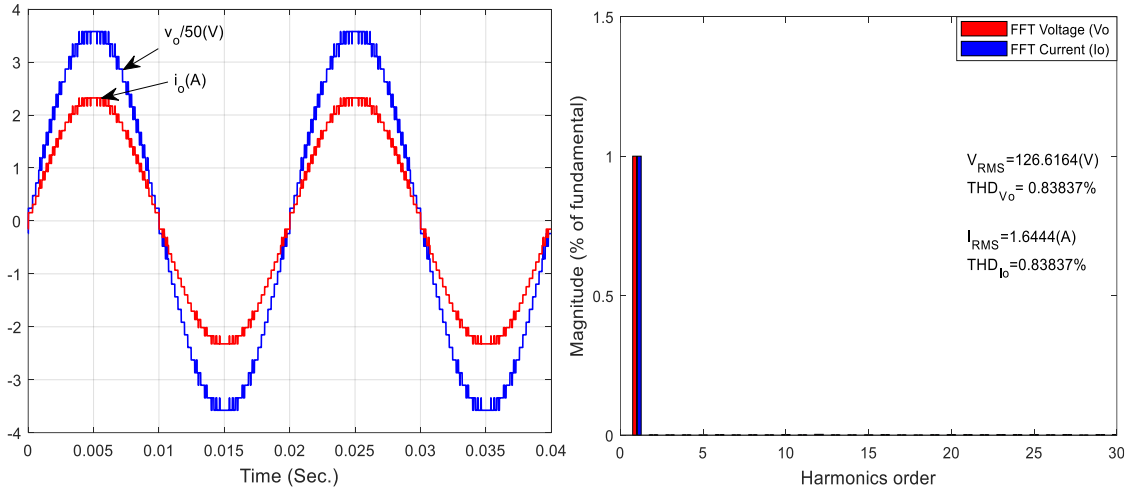


(a) R-Load

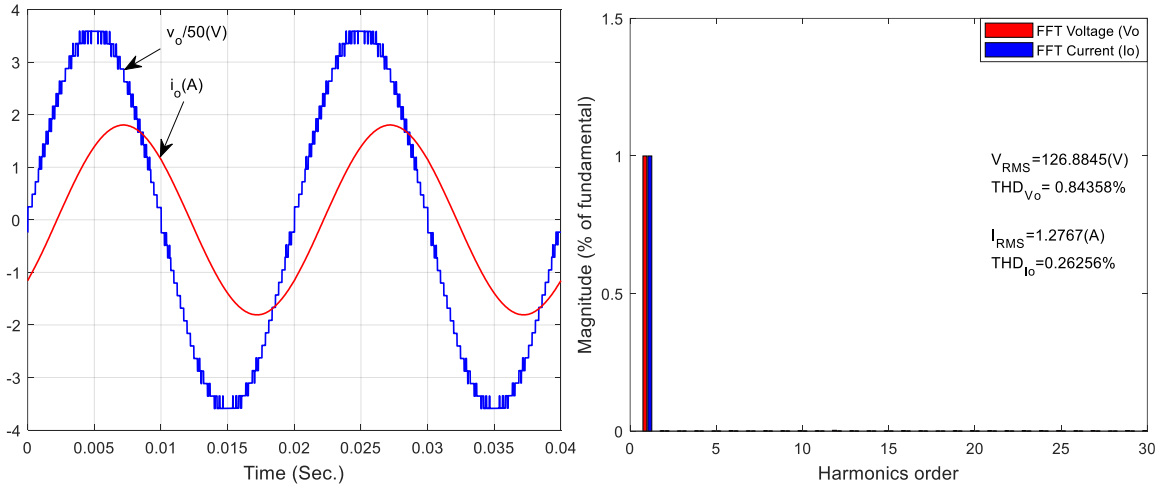


(b) RL-Load

Figure 4 Model outcomes of the 31-level output voltage and current and its FFT analysis based on MASPWM technique and WZ state (a) R-Load (b) RL-Load

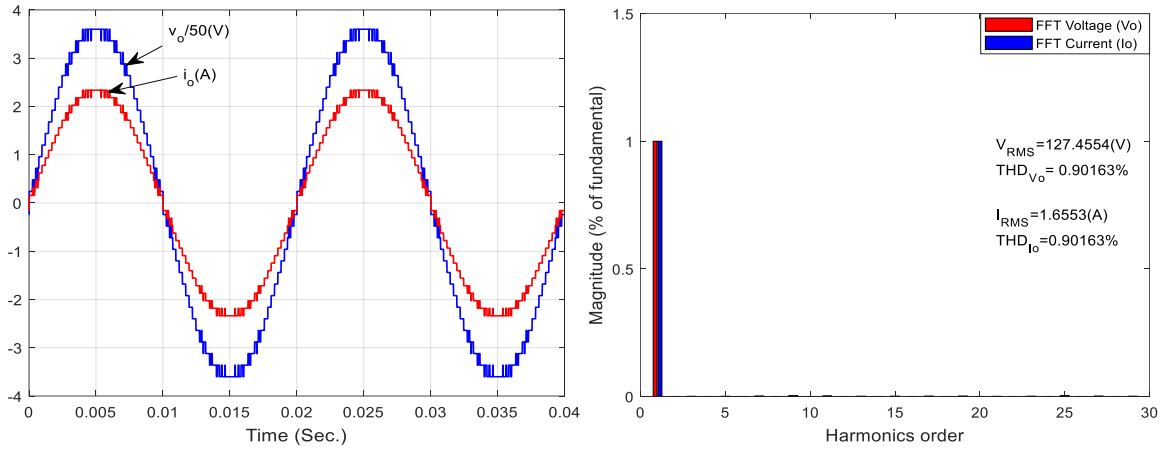


(a) R-Load

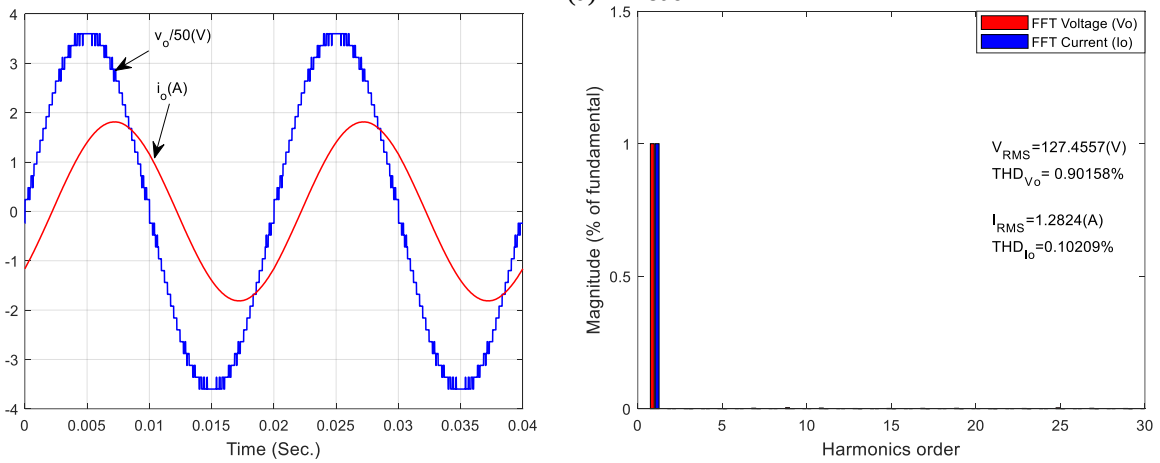


(b) RL-Load

Figure 5 Model outcomes of the 31-level output voltage and current and its FFT analysis based on PDLSPWM technique and WoZ state (a) R-Load (b) RL-Load

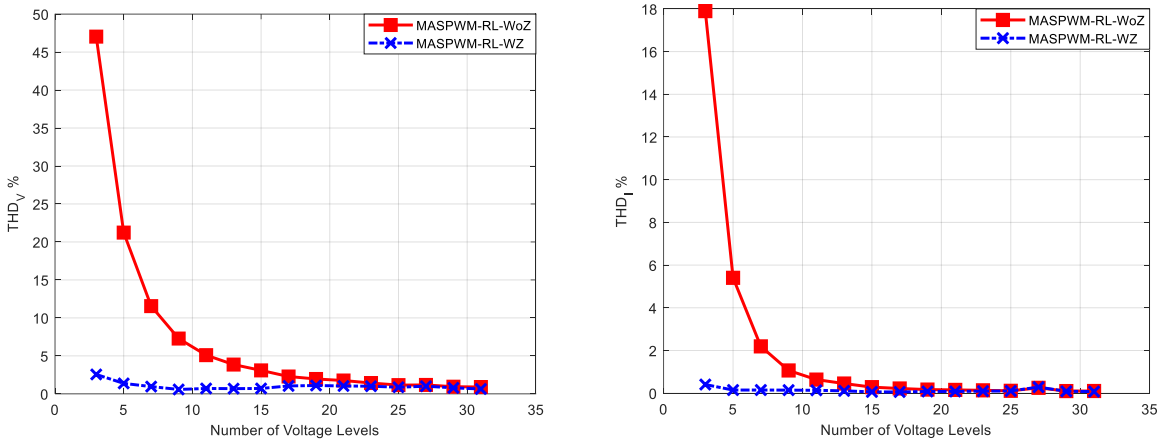


(a) R-Load



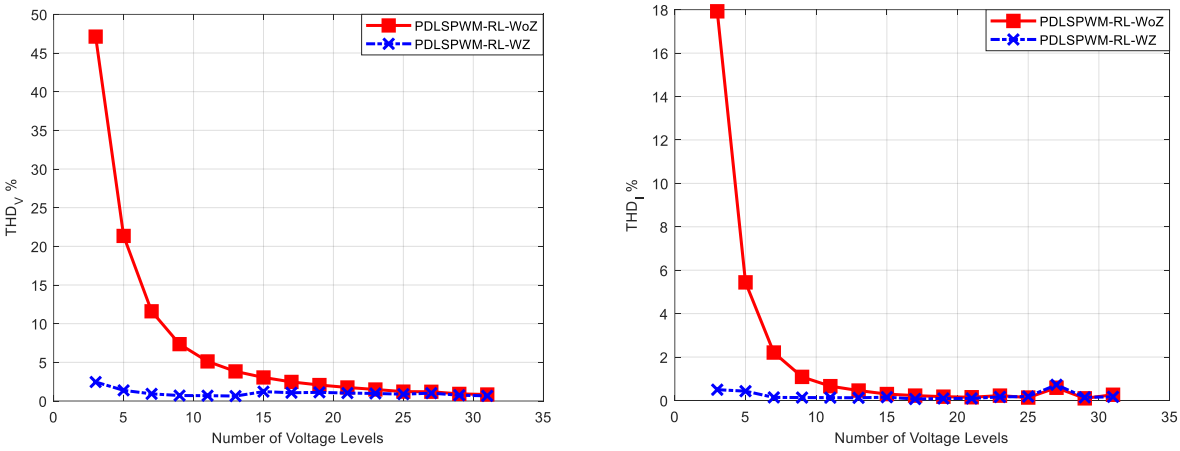
(b) RL-Load

Figure 6 Model outcomes of the 31-level output voltage and current and its FFT analysis based on MASPWM technique and WoZ state (a) R-Load (b) RL-Load



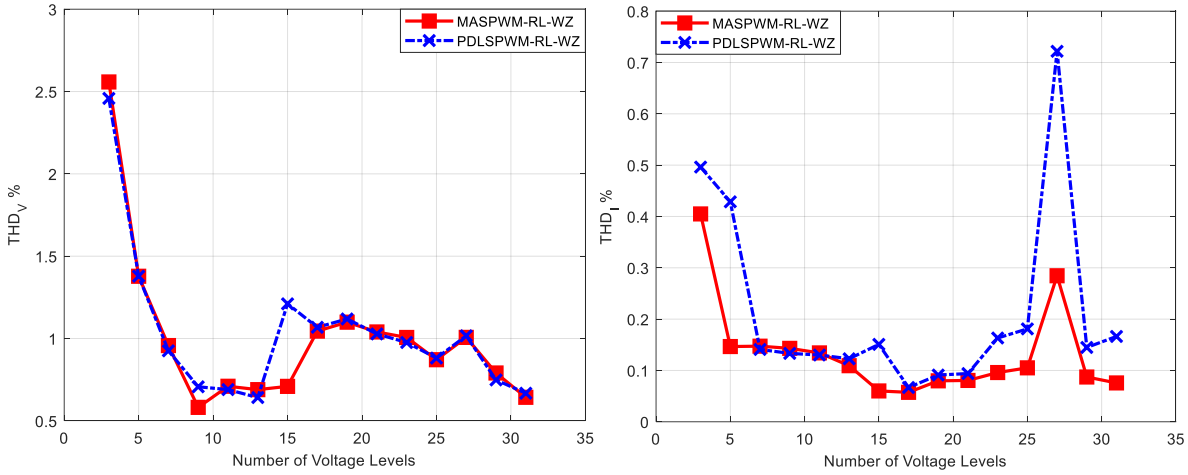
(a) (b)

Figure 7 The THD waveform of the MI: (a) voltage and (b) current based on MASPWM using WZ and WoZ cases



(a) (b)

Figure 8 The THD waveform of the MI: (a) voltage and (b) current based on PDLSPWM using WZ and WoZ cases



(a) (b)

Figure 9 The THD waveform of the MI: (a) voltage and (b) current using PDLSPWM and MASPWM techniques at WZ case

Table 2 Comparison of 31-level circuit with related MI topologies

Ref.	SW	ND	NPE	NDC	SDC	THDV	THDI
[54]	14	-	14	4	(1:2:4:8) Vdc	3.35%	3.35%
[59]	8	4	12	4	(1:2:4:8) Vdc	2.83%	2.83%
[60]	12	-	12	4	(1:2:4:8) Vdc	10.22%	10.22%
[61]	10	-	10	4	(1:2:5:10) Vdc	3.62%	3.71%
Proposed circuit (PDLSPWM-WZ)	10	-	10	4	(1:2:5:10) Vdc	0.667%	0.166%
Proposed circuit (MASPWM-WZ)	10	-	10	4	(1:2:5:10) Vdc	0.643%	0.075%

5.Conclusion and future work

A MI with ten SWs and four DCSs was proposed to evaluate the efficacy of this circuit configuration using MASPWM and PDLSPWM controller techniques during both WZ and WoZ states. The configuration of the 4-DC sources was set at (1:2:5:10) Vdc. By reducing the number of SWs and sources compared to traditional models, initial setup costs are minimized and operational efficiency is enhanced. The analysis revealed that the MASPWM controller in WZ state produced lower THD values than other states. The modeling results confirm the effectiveness of the proposed circuit and controller in generating output voltages that meet IEEE standards, as evidenced by the lower THD values in the WZ state compared to the WoZ state. Specifically, the highest THD values recorded using the PDLSPWM technique were 0.8435% and 0.2625%, respectively, for output voltage and current. Meanwhile, the MASPWM technique achieved maximum THD values of 0.90158% and 0.10209%, respectively. These findings indicate that the designed controllers and suggested power circuit perform well in delivering the required output voltage levels with minimal THD.

The study focused solely on a 31-level inverter; however, further research could explore increasing the output voltage levels. Future work may involve practical testing of the system with inputs powered by RESs. Additionally, a sensorless speed and torque control-based AC motor could be modeled as a dynamic load. This circuit can be enhanced by considering additional factors to make the system as comprehensive as possible.

Acknowledgment

None.

Conflicts of interest

The authors have no conflicts of interest to declare.

Data availability

None.

Author's contribution statement

The author confirms sole responsibility for the following: study conception and design, data collection, analysis and interpretation of results, and manuscript preparation.

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Appendix I

S.No.	Abbreviation	Description
1	AC	Alternating Current
2	AMI	Asymmetrical MI
3	CHMI	Cascaded H-bridge MI
4	DC	Direct Current
5	MASPWM	Modified Absolute Sinusoidal Pulse Width Modulation
6	MI	Multilevel Inverter
7	ND	Number of Diodes
8	NDC	Number of Voltage Sources
9	NPE	Total Number of Power Electronics Devices
10	PDLSPWM	Phase Disposition, Level-Shifted Pulse Width Modulation
11	PV	Photovoltaic
12	PWM	Pulse Width Modulation
13	RES	Renewable Energy Source
14	SDC	Structure of DC Voltages
15	SMI	Symmetrical MI
16	SW	Power Switches
17	THD	Total Harmonic Distortion
18	THDI	THD of the Output Current
19	THDV	THD of the Output Voltage
20	Vdc	Volts of Direct Current
21	WoZ	Without Zero Level State
22	WZ	With Zero Level State